

# CPRI Specification V1.4 (2006-03-31)

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*Interface Specification*

## **Common Public Radio Interface (CPRI); Interface Specification**

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# 1. Introduction

The Common Public Radio Interface (CPRI) is an industry cooperation aimed at defining a publicly available specification for the key internal interface of radio base stations between the Radio Equipment Control (REC) and the Radio Equipment (RE). The parties cooperating to define the specification are Ericsson AB, Huawei Technologies Co. Ltd, NEC Corporation, Nortel Networks SA and Siemens AG.

## Motivation for CPRI:

The CPRI specification enables flexible and efficient product differentiation for radio base stations and independent technology evolution for Radio Equipment (RE) and Radio Equipment Control (REC).

## Scope of Specification:

The necessary items for transport, connectivity and control are included in the specification. This includes User Plane data, Control and Management Plane transport mechanisms, and means for synchronization.

A focus has been put on hardware dependent layers (layer 1 and layer 2). This ensures independent technology evolution (on both sides of the interface), with a limited need for hardware adaptation. In addition, product differentiation in terms of functionality, management, and characteristics is not limited.

The specification will have the following scope:

1. A digitized and serial internal radio base station interface between 'Radio Equipment Control' (REC) and 'Radio Equipment' (RE) will be specified.
2. Three different information flows (User Plane data, Control and Management Plane data, Synchronization Plane data) will be multiplexed over the interface.
3. The Specification will cover Layers 1 and 2.
  - 3a. The physical layer (layer 1) will support both an electrical interface (e.g., what is used in traditional radio base stations), and an optical interface (e.g. for radio base stations with remote radio equipment).
  - 3b. Layer 2 will support flexibility and scalability.
- The specification shall comply with 3GPP UTRA FDD release 6.

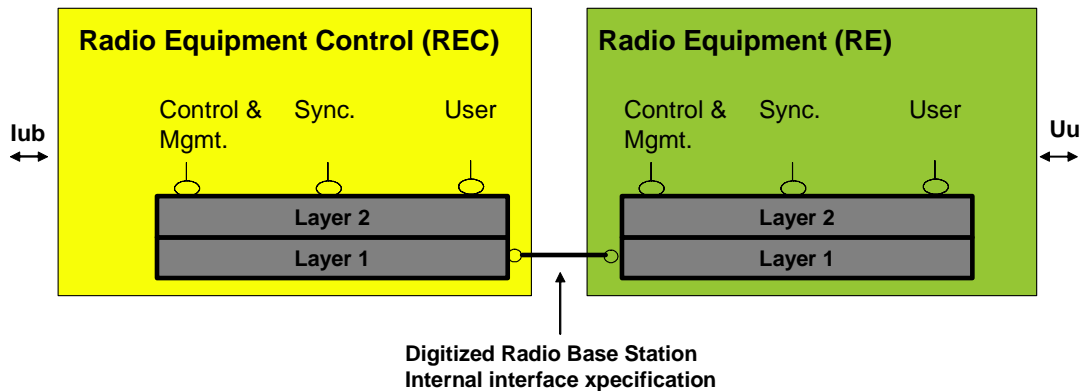


Figure 1: System and Interface Definition

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## 2. System Description

This chapter describes the CPRI related parts of the basic radio base station system architecture and defines the mapping of the functions onto the different subsystems. Furthermore, the reference configurations and the basic nomenclature used in the following chapters will be defined.

The following description will be based on the UMTS (Universal Mobile Telecommunication System) nomenclature, because this is the first mobile radio standard the Common Public Radio Interface (CPRI) specification supports. However, the interface may also be used for other radio standards.

### 2.1. Definitions/Nomenclature

This section provides the basic nomenclature that will be used in the following chapters.

#### **Subsystems:**

The radio equipment control and the radio equipment are described in the following chapter.

#### **Protocol layers:**

This specification defines the protocols for the physical layer (layer 1) and the data link layer (layer 2).

Layer 1 defines:

- Electrical characteristics
- Optical characteristics
- Time division multiplexing of the different data flows
- Low level signalling

Layer 2 defines:

- Media access control
- Flow control
- Data protection of the control and management information flow

#### **Protocol data planes:**

The following data flows can be discerned:

Control Plane:	Control data flow used for call processing.
Management Plane:	Management information for the operation, administration and maintenance of the CPRI link and the RE.
User Plane:	Data that has to be transferred from the radio base station to the mobile station and vice versa. These data are transferred in the form of IQ data.
Synchronization:	Data flow which transfers synchronization and timing information between REC and RE.

The control and management plane will be mapped to a single information flow over the CPRI link.

#### **User plane data:**

The user plane data are transported in the form of IQ data. Several IQ data flows will be sent via one physical CPRI link. Each IQ data flow reflects the data of one antenna for one carrier, the so-called antenna-carrier (AxC).

#### **Antenna-carrier (AxC):**

One antenna-carrier is the amount of digital baseband (IQ) U-plane data necessary for either reception or transmission of one UTRA-FDD carrier at one independent antenna element.

#### **AxC Container:**

It contains the IQ samples of one AxC for one UMTS chip duration.

### Service Access Points:

For all protocol data planes layer 2 services access points are defined that will be used as reference points for performance measurements. These service access points will be denoted as  $SAP_{CM}$ ,  $SAP_S$  and  $SAP_{IQ}$  as illustrated in Figure 2

### Downlink:

Direction from REC to RE.

### Uplink:

Direction from RE to REC.

## 2.2. System Architecture

Future radio base stations should provide deployment flexibility for the mobile network operators, i.e., in addition to a concentrated radio base station, more flexible radio base station system architectures involving remote radio equipment shall be supported. This can be achieved by a decomposition of the radio base station into two basic building blocks, the so-called radio equipment control (REC) and the radio equipment (RE) itself. Both parts may be physically separated (i.e., the RE may be close to the antenna, whereas the REC is located in a conveniently accessible site) or both may be co-located as in a conventional radio base station design.

The radio equipment control provides access to the Radio Network Controller via the Iub interface (for the UMTS radio access network), whereas the radio equipment serves as the air interface to the user equipment (in an UMTS network this is called the Uu interface). The REC comprises the radio functions of the digital baseband domain, whereas the RE contains the analogue radio frequency functions. The functional split between both parts is done in such a way that a generic interface based on In-Phase and Quadrature (IQ) data can be defined. A more detailed description of the functional split between both parts of an UMTS system is provided in Section 2.4.

In addition to the user plane data (IQ data), control and management as well as synchronization signals have to be exchanged between the REC and the RE. All information flows will be multiplexed onto a digital serial communication line using appropriate layer 1 and layer 2 protocols. The different information flows will have access to the layer 2 via appropriate service access points (SAPs). This defines the common public radio interface illustrated in Figure 2.

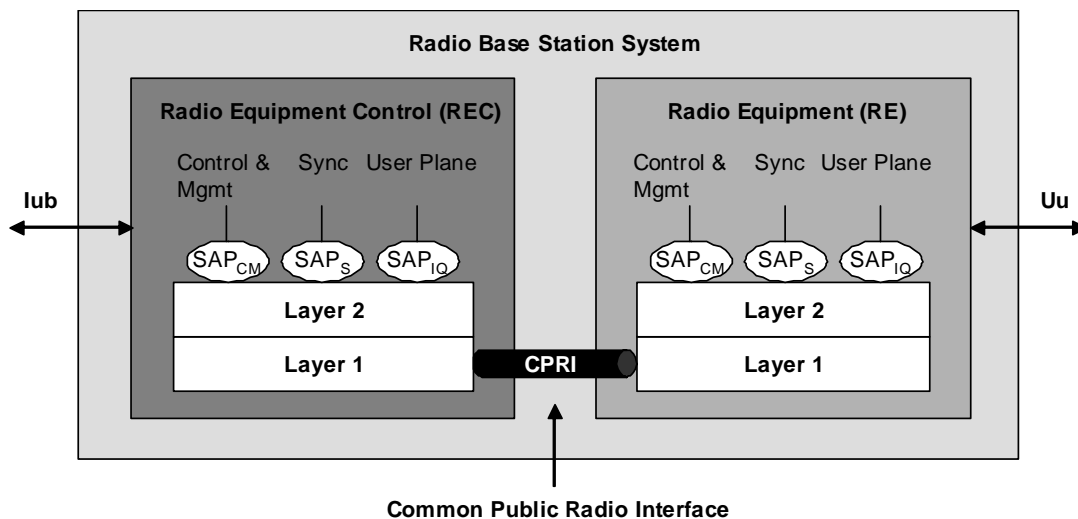


Figure 2: Basic System Architecture and Common Public Radio Interface Definition

## 2.3. Reference Configurations

This section provides the reference configurations that have to be supported by the CPRI specification. The basic configuration, shown in Figure 3, is composed of one REC and one RE connected by a single CPRI physical link. The basic configuration can be extended in several ways:

- First, several CPRI physical links can be used to enhance the system capacity as required for large system configurations involving many antennas and carriers (see Figure 4). This extension of the specification is straightforward if it is assumed that an IQ data flow of a certain antenna and a certain antenna-carrier (see Section 2.1) is carried by one CPRI link and is not distributed over several CPRI links. Therefore, the number of physical links is not restricted by this specification.
- Second, several radio equipment entities may be served by one REC as illustrated in Figure 5.



Figure 3: Single point-to-point link between one REC and one RE

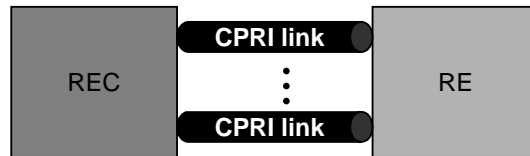


Figure 4: Multiple point-to-point links between one REC and one RE

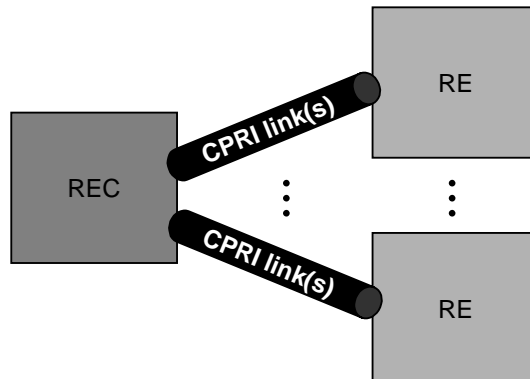


Figure 5: Multiple point-to-point links between one REC and several REs

## 2.4. Functional Description

This section provides a more detailed view on the functional split between REC and RE for the UMTS standard, which provides the basis for the requirement definition in the next chapter.

Basically, the REC is concerned with the Iub transport, the radio base station control and management as well as the digital baseband processing. The radio equipment provides the analogue and radio frequency functions such as filtering, modulation, frequency conversion and amplification. An overview on the functional separation between REC and RE is given in Table 1.

Table 1: Functional decomposition between REC and RE (valid for the UMTS FDD standard)

Functions of REC		Functions of RE	
Downlink	Uplink	Downlink	Uplink
Radio base station control & management			
Iub transport		RRC Channel Filtering	
Iub Frame protocols		D/A conversion	A/D conversion
Channel Coding	Channel De-coding	Up Conversion	Down Conversion
Interleaving	De-Interleaving	ON/OFF control of each carrier	Automatic Gain Control
Spreading	De-spreading	Carrier Multiplexing	Carrier De-multiplexing
Scrambling	De-scrambling	Power amplification and limiting	Low Noise Amplification
Adding of physical channels	Signal distribution to signal processing units	Antenna supervision	
Transmit Power Control of each physical channel	Transmit Power Control & Feedback Information detection	RF filtering	RF filtering
Frame and slot signal generation (including clock stabilization)			
Measurements		Measurements	



## 3. Interface Baseline

This chapter provides an overview on the basic input requirements for the CPRI specification. The requirements are to be met by the CPRI specification, and will be used as baseline for future enhancements of the CPRI interface specification. Note that this chapter does not specify the requirements on a CPRI compliant device (see chapter 5.2) but expresses the superset of requirements on an interface from all expected applications using the CPRI interface.

### 3.1. Supported Radio Standards

The interface shall support transmission of all necessary data between REC and RE in both directions for a radio base station consisting of one REC and one or more REs compliant to the following radio standards:

Requirement No.	Requirement Definition	Requirement Value
R-1	Radio Standard and Release	3GPP UTRA FDD, Release 6, December 2005

The support of other standards is not required in this release of the CPRI specification, but the future use of the interface for other standards shall not be precluded.

### 3.2. Operating Range

The interface shall support a continuous range of distances (i.e., cable lengths) between REC and RE. The minimum required range is defined by the cable length in the following table:

Requirement No.	Requirement Definition	Requirement Value
R-2	Cable length (lower limit)	0 m
R-3	Cable length (upper limit)	>10 km

The interface shall support one cable for uplink and downlink with separate transmission media (e.g., optical fibres) for uplink and downlink. Simplex operation shall be supported per transmission medium (e.g., optical fibres).

### 3.3. Topology/Switching/Multiplexing

The following topologies shall be supported by the CPRI specification:

Requirement No.	Requirement Definition	Requirement Value
R-4	Topology	Star topology, i.e., one REC with one or several REs

The support of other topologies is not required in this release of the specification, but the use of the interface in other topologies shall not be precluded.

The connection of one RE to more than one REC is not considered.

## 3.4. Bandwidth/Capacity/Scalability

### 3.4.1. Capacity in terms of Antenna-Carriers

The capacity of one interface link shall be expressed in terms of UTRA-FDD-antenna-carriers (abbreviation: "antenna-carrier" or "AxC"). One UTRA-FDD-antenna-carrier is the amount of digital baseband (IQ) U-plane data necessary for either reception or transmission of one UTRA-FDD carrier at one independent antenna element. One antenna element is typically characterized by having exactly one antenna connector to the RE.

CPRI shall be defined in such a way that the following typical Node B configurations can be supported:

- 1 RE supports one sector
  - Up to 4 carriers x 1 antenna per RE (e.g. 6 REs for 3 sectors).
  - Up to 4 carriers x 2 antennas per RE (e.g. 3 REs for 3 sectors)
- 1 RE supports 3 sectors
  - From 1 to 4 carriers x 2 antennas x 3 sectors per RE

Therefore, the following number of AxC shall be supported by the CPRI specification:

Requirement No.	Requirement Definition	Requirement Value
R-5	Number of antenna carriers per physical line	4
R-6	Number of antenna carriers per physical line	6
R-7	Number of antenna carriers per physical line	8
R-8	Number of antenna carriers per physical line	12
R-9	Number of antenna carriers per physical line	18
R-10	Number of antenna carriers per physical line	24

### 3.4.2. Required U-plane IQ Sample Widths

The uplink IQ sample widths supported by the CPRI specification shall be between 4 and 10 bits for I and Q each, and the downlink IQ sample widths supported by the CPRI specification shall be between 8 and 20 bits for I and Q each.

Requirement No.	Requirement Definition	Requirement Value
R-11	Minimum uplink IQ sample width	4
R-12	Maximum uplink IQ sample width	10
R-13	Minimum downlink IQ sample width	8
R-14	Maximum downlink IQ sample width	20

Notes:

- Oversampling Factor of 2 or 4 in uplink and 1 in downlink is assumed
- Automatic Gain Control is assumed in uplink

### 3.4.3. Required C&M-plane Bit Rate

The interface shall support a minimum bit rate for the for the M-plane transmission per RE:

Requirement No.	Requirement Definition	Requirement Value
R-15	Minimum transmission rate of M-plane data (layer 1)	200 kbit/s

Additionally, the interface shall support a minimum bit rate for the transmission of C-plane data per AxC:

Requirement No.	Requirement Definition	Requirement Value
R-16	Minimum transmission rate of C-plane data (layer 1)	25 kbit/s

The overhead on layer 2 due to frame delineation and frame check sequence depends on the frame length determined by higher layers. Assuming this overhead is well below 20%, a minimum net bit rate of 20kbit/s per AxC is available at the service access point  $SAP_{CM}$  as shown in Figure 2.

## 3.5. Synchronization/Timing

### 3.5.1. Frequency Synchronization

The interface shall enable the RE to achieve the required frequency accuracy of  $\pm 0.05$ ppm (3GPP TS 25.104 [ 8 ] section 6.3). The central clock for frequency generation in the RE shall be synchronized to the bit clock of the interface. With 8B/10B line coding the bit clock rate of the interface shall be a multiple of 38.4MHz in order to allow a simple synchronization mechanism and frequency generation in the RE.

The impact of jitter on the frequency accuracy budget of the interface to the radio base station depends on the cut-off frequency of the RE synchronization mechanism. The interface shall accommodate a synchronization mechanism cut-off frequency high enough so that a standard crystal oscillator suffices as master clock of the RE. The contribution  $\Delta f / f_0$  of the jitter  $\tau$  to the frequency accuracy shall be defined with the cut-off frequency  $f_c$  as follows:

$$\frac{\Delta f}{f_0} = \frac{1}{f_0} \cdot \sqrt{\int_0^{f_c} f^2 \cdot 2 \cdot 10^{\frac{L(f)}{10dB}} \cdot df}, \quad (1)$$

where  $L(f)$  is the single-side-band phase noise in dBc/Hz acquired on the interface with the following relation to the jitter  $\tau$  :

$$\tau = \frac{1}{2 \cdot \pi \cdot f_0} \cdot \sqrt{\int_0^{f_0/2} 2 \cdot 10^{\frac{L(f)}{10dB}} \cdot df} \quad (2)$$

The reference point for the jitter and phase noise specification is a stable clock signal at the service access point SAP<sub>S</sub> as shown in Figure 2. The frequency of this clock signal is denoted as  $f_0$ .

With  $f_c$  in equation (1) being the maximum allowed cut-off frequency, the impact of jitter on the radio base station frequency accuracy budget shall meet the following requirements:

Requirement No.	Requirement Definition	Requirement Value
R-17	Maximum allowed cut-off frequency $f_c$ of RE synchronization	300 Hz
R-18	Maximum contribution $\Delta f / f_0$ of jitter on the interface to the radio base station frequency accuracy budget (between REC SAP <sub>S</sub> and RE SAP <sub>S</sub> )	$\pm 0.002$ ppm

### 3.5.2. Frame Timing Information

The synchronization part of the interface shall include mechanisms to provide precise frame timing information from the REC to the RE. The frame timing information can be recovered on the RE in order to achieve the timing accuracy requirements as described in the sections below. The frame timing information is allocated to the service access point SAP<sub>S</sub> as shown in Figure 2. Timing accuracy and delay accuracy as required in the subsections below refer to the accuracy of timing signals at the service access point SAP<sub>S</sub>. These timing signals shall be used in the RE for the precise timing of RF signal transmission and reception on the air interface.

### 3.5.3. Absolute Timing Accuracy

The interface shall enable a radio base station to meet the requirement "time alignment error in Tx Diversity shall not exceed  $\frac{1}{4} T_c$ " (3GPP TS 25.104 [ 8 ] section 6.8.4) even when both TX signals are transmitted via different REs. In order to meet the relative delay accuracy between REs in a star topology, absolute delays for REC and RE have to be specified.

The interface shall also support "UTRAN GPS Timing of Cell Frames for UE positioning" (3GPP TS 25.133 [ 9 ] section 9.2.10), which requires absolute delay accuracy.

The absolute delay accuracy on one interface link excluding the group delay on the transmission medium, i.e. excluding the cable length, shall meet the following requirement.

Requirement No.	Requirement Definition	Requirement Value
R-19	Absolute delay accuracy excluding the cable length	$\pm T_c / 32$

### 3.5.4. Round Trip Delay Accuracy

The interface shall enable a radio base station to meet the requirement "round trip time absolute accuracy  $\pm 0.5 T_c$ " (3GPP TS 25.133 [ 9 ] section 9.2.8.1).

The round trip time absolute accuracy of the interface, excluding the round trip group delay on the transmission medium (i.e., excluding the cable length), shall meet the following requirement.

Requirement No.	Requirement Definition	Requirement Value
R-20	Round trip absolute accuracy excluding cable length	$\pm T_c/16$

### 3.6. Delay Calibration

The interface shall enable periodic measurement of the cable length, i.e., measurement of the round trip group delay on the transmission medium. The measurement results shall be available on the REC in order to meet the following requirements without the need to input the cable length to the REC by other means:

- “time alignment error in Tx Diversity shall not exceed  $\frac{1}{4} T_c$ ” (3GPP TS 25.104 [ 8 ] section 6.8.4)
- “round trip time absolute accuracy  $\pm 0.5 T_c$ ” (3GPP TS 25.133 [ 9 ] section 9.2.8.1)
- “UTRAN GPS Timing of Cell Frames for UE positioning” (3GPP TS 25.133 [ 9 ] section 9.2.10)

The accuracy of the measurement of round trip group delay on the transmission medium shall meet the following requirement:

Requirement No.	Requirement Definition	Requirement Value
R-21	Accuracy of the round trip delay measurement of the link	$\pm T_c/16$

### 3.7. Link Maintenance

The layer 1 of the interface shall be able to detect and indicate loss of signal (LOS) and loss of frame including frame synchronization (LOF). A remote alarm indication (RAI) shall be returned to the sender on layer 1 as a response to these errors. In addition the SAP defect indication (SDI) shall be sent to the remote end when any of the SAPs is not valid due to an equipment error.

The signals

- LOS
- LOF
- SDI
- RAI

shall be handled on layer 1 and shall also be available to the higher layers of the interface.

Requirement No.	Requirement Definition	Requirement Value
R-22	Loss of Signal (LOS) detection and indication	-
R-23	Loss of Frame (LOF) detection and indication	-
R-24	SAP Defect Indication (SDI)	-
R-25	Remote Alarm Indication (RAI)	-

## 3.8. Quality of Service

### 3.8.1. Maximum Delay

In order to support efficient implementation of inner loop power control the absolute round trip time for U-plane data (IQ data) on the interface, excluding the round trip group delay on the transmission medium (i.e. excluding the cable length), shall not exceed the following maximum value:

Requirement No.	Requirement Definition	Requirement Value
R-26	Maximum absolute round trip delay excluding cable length	5 $\mu$ s

Round trip time shall be defined as the downlink delay plus the uplink delay. The delay shall be precisely defined as the time required transmitting a complete IQ-sample over the interface. The availability and validity of an IQ-sample shall be defined at the service access point  $SAP_{IQ}$  as shown in Figure 2. The precise point of time of availability and validity shall be indicated by the edge of an associated clock signal at the service access point  $SAP_{IQ}$ . The delay (e.g. in downlink) is defined as the time difference between the edge at the input  $SAP_{IQ}$  (e.g. on REC) and the edge at the output  $SAP_{IQ}$  (e.g. on RE).

### 3.8.2. Bit Error Ratio U-plane

The interface shall provide U-plane data transmission (on layer 1) with a maximum bit error ratio as specified below:

Requirement No.	Requirement Definition	Requirement Value
R-27	Maximum bit error ratio (BER) of U-plane	$10^{-12}$

It should be a design goal to avoid forward error correction on layer 1 to achieve a cost efficient solution. There shall not be any data protection on layer 2.

### 3.8.3. Bit Error Ratio C&M-plane

The interface shall provide C&M-plane data transmission with a maximum bit error ratio (on layer 1) as specified below:

Requirement No.	Requirement Definition	Requirement Value
R-28	Maximum bit error ratio (BER) of C&M-plane	$10^{-12}$

Additionally, a frame check sequence (FCS) shall be provided for C&M-plane data bit error detection on layer 2. The minimum length of the frame check sequence is defined in the following table:

Requirement No.	Requirement Definition	Requirement Value
R-29	Minimum length of frame check sequence (FCS)	16 bit

## 3.9. Start-up Requirement

### 3.9.1. Clock Start-up Time Requirement

CPRI shall enable the RE clock to achieve synchronization with respect to frequency accuracy and absolute frame timing accuracy within 10 seconds.

Requirement No.	Requirement Definition	Requirement Value
R-30	Maximum clock synchronization time	10 s

### 3.9.2. Plug and Play Requirement

CPRI shall support auto-negotiation for selecting the line bit rate.

Requirement No.	Requirement Definition	Requirement Value
R-31	Auto-negotiation of line bit rate	-

CPRI shall support auto-negotiation for selecting the C&M-plane type and bit rate (layer 1).

Requirement No.	Requirement Definition	Requirement Value
R-32	Auto-negotiation of C&M-plane type and bit rate (layer 1)	-

## 4. Interface Specification

### 4.1. Protocol Overview

CPRI defines the layer 1 and layer 2 protocols for the transfer of user plane, C&M as well as synchronization information between REC and RE. The interface shall support the following types of information flows:

- IQ Data: User plane information in the form of in-phase and quadrature modulation data (digital baseband signals).
- Synchronization: Synchronization data used for frame and time alignment.
- L1 Inband Protocol: Signalling information that is related to the link and is directly transported by the physical layer. This information is required, e.g. for system start-up, layer 1 link maintenance and the transfer of time critical information that has a direct time relationship to layer 1 user data.
- C&M data: Control and management information exchanged between the control and management entities within the REC and the RE. This information flow is given to the higher protocol layers.
- Protocol Extensions: This information flow is reserved for future protocol extensions. It may be used to support, e.g., more complex interconnection topologies or other radio standards.
- Vendor Specific Information: This information flow is reserved for vendor specific information.

The user plane information is sent in the form of IQ data. The IQ data of different antenna carriers are multiplexed by a time division multiplexing scheme onto an electrical or optical transmission line. The control and management data are either sent as inband protocol (for time critical signalling data) or by layer 3 protocols (not defined by CPRI) that reside on top of appropriate layer 2 protocols. Two different layer 2 protocols for C&M data – subset of High level Data Link Control (HDLC) and Ethernet – are supported by CPRI. These additional control and management data are time multiplexed with the IQ data. Finally, additional time slots are available for the transfer of any type of vendor specific information. Figure 6 provides an overview on the basic protocol hierarchy.

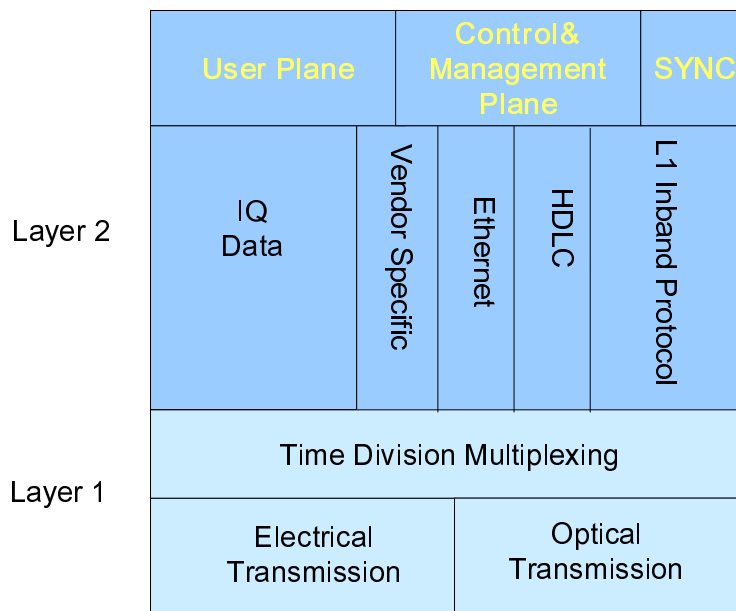


Figure 6: CPRI protocol overview



## 4.2. Physical Layer (Layer 1) Specification

### 4.2.1. Line Bit Rate

In order to achieve the required flexibility and cost efficiency, three different line bit rates have been defined. Therefore, the CPRI line bit rate can be selected from the following option list:

- CPRI line bit rate option 1: 614.4 Mbit/s
- CPRI line bit rate option 2: 1228.8 Mbit/s (2 x 614.4 Mbit/s)
- CPRI line bit rate option 3: 2457.6 Mbit/s (2 x 1228.8 Mbit/s)

It is mandatory that each REC and RE support at least one of the above cited CPRI line bit rates.

All CPRI line bit rates have been chosen in such a way that the basic UMTS chip rate of 3.84 Mbit/s can be recovered in a cost-efficient way from the line bit rate taking into account the 8B/10B line coding defined in Section 4.2.5. For example, the 1228.8 Mbit/s correspond to an encoder rate of 122.88 MHz for the 8B/10B encoder and a subsequent frequency division by a factor of 32 provides the basic UMTS chip rate.

### 4.2.2. Physical Layer Modes

CPRI is specified for several applications with different interface data rates and REC to RE ranges. The table below defines several CPRI physical layer modes:

Table 2: CPRI physical layer modes

Data rate	Electrical	Optical	
		Short range	Long range
614.4 Mbit/s	E.6	OS.6	OL.6
1228.8 Mbit/s	E.12	OS.12	OL.12
2457.6 Mbit/s	E.24	OS.24	OL.24

For each of those CPRI “modes” the layer one shall fulfil the requirements as specified in Section 3.5 (clock stability and noise) and Sections 3.8.2 and 3.8.3 ( $BER < 10^{-12}$ ).

Two electrical variants are recommended for CPRI usage, denoted HV (high voltage) and LV (low voltage) in Figure 6A below. The HV variant is guided by IEEE 802.3-2002 [ 1 ], clause 39 (1000base-CX) but with 100 ohm impedance. The LV variant is guided by IEEE 802.3ae-2002 [ 2 ] clause 47 (XAUI) but with lower bit rate. See annex 6.2 for more details on the adaptation to CPRI line bit rates and applications.

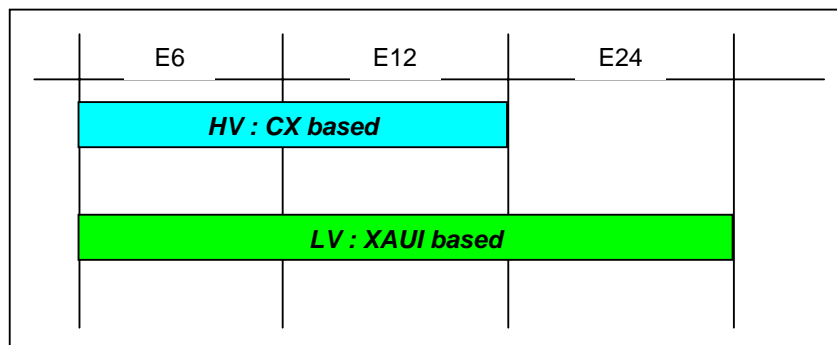


Figure 6A: HV (high voltage) and LV (low voltage) electrical layer 1 usage

It is recommended to reuse optical transceivers from the following High Speed Serial Link standards:

- Gbit Ethernet: Standard IEEE 802.3-2002 [ 1 ] clause 38 (1000BASE-SX/LX)
- 10 Gbit Ethernet: Standard IEEE 802.3ae-2002 [ 2 ] clause 53 (10GBASE-LX4)
- Fiber channel (FC-PI) – Standard INCITS 352 [ 3 ]
- Infiniband Volume 2 Rel 1.1 (November 2002) [ 6 ]

It is recommended to use an optical solution allowing for reuse of SERDES components supporting the HV and/or LV electrical variants.

The specification does not preclude the usage of any other technique that is proven to reach the same BER performance ( $BER < 10^{-12}$ ) and clock stability for the dedicated CPRI application.

CPRI clock tolerance is driven by 3GPP requirements (see 3GPP TS 25.104 [ 8 ]), which fully enable usage of existing high speed serial link standards.

### 4.2.3. Electrical Interface

#### 4.2.3.1. Electrical Cabling

No specific cabling is recommended by CPRI.

The cable performance shall be such that transmitter and receiver performance required in section 3 are fulfilled. See also annex 6.2 for implicit recommendations on electrical characteristics.

#### 4.2.3.2. Electrical Connectors

CPRI electrical implementation may use connector solutions that are described and defined in INCITS 352 (Fiber channel FC-PI) [ 3 ] or IEEE Std 802.3-2002 [ 1 ].

These solutions are known to achieve the performance required in section 3. See also annex 6.2 for implicit recommendations on electrical characteristics.

### 4.2.4. Optical Interface

#### 4.2.4.1. Optical Cabling

The cable performance shall be such that transmitter and receiver performance required in section 3 are fulfilled. The fiber cables recommended for CPRI are:

- IEC 60793-2:2002.Type A1a (50/125  $\mu\text{m}$  multimode) [ 4 ]
- IEC 60793-2:2002.Type A1b (62.5/125  $\mu\text{m}$  multimode) [ 4 ]
- IEC 60793-2 :2002.Type B1 (10/125  $\mu\text{m}$  single-mode) [ 5 ]

The exception characteristic as specified in IEEE Std 802.3-2002 [ 1 ] Table 38-12 and IEEE Std 802.3ae-2002 [ 2 ] Table 53-14 may be taken into account.

#### 4.2.4.2. Optical Connectors

CPRI optical implementation may use connector solutions that are described and defined in INCITS 352 [ 3 ] (Fiber channel FC-PI) or IEEE Std 802.3-2002 [ 1 ].

These solutions are known to achieve the performance required in section 3. A high flexibility in the choice of connector and transceiver can be achieved by adopting the SFP building practice.

### 4.2.5. Line Coding

8B/10B line coding shall be used for serial transmission according to IEEE Standard 802.3-2002 [ 1 ].

## 4.2.6. Bit Error Correction/Detection

The physical layer has been designed in such a way that a very low bit error ratio can be achieved without expensive forward error corrections schemes (see requirement R-27). Therefore, no general bit error correction shall be applied at layer 1. Some layer 1 control bits have their own protection, see chapter 4.2.7.6.2. The RE and the REC shall support detection of 8B/10B code violations. Link failures shall be detected by means of 8B/10B code violations.

## 4.2.7. Frame Structure

### 4.2.7.1. Basic Frame Structure

#### 4.2.7.1.1. Framing Nomenclature

The length of a basic frame is  $1 T_C = 1/3.84 \text{ MHz} = 260.416667\text{ns}$ . A basic frame consists of 16 words with index  $W=0\dots15$ . The word with the index  $W=0$ , 1/16 of the basic frame, is used for one control word. The length  $T$  of the word depends on the CPRI line bit rate as shown in Table 3. Each bit within a word can be addressed with the index  $B$ , where  $B=0$  is the LSB and  $B=T-1$  is the MSB. Each BYTE within a word can be addressed with the index  $Y$ , where  $B=0$  is LSB of  $Y=0$ ,  $B=7$  is MSB of  $Y=0$ ,  $B=8$  is LSB of  $Y=1$ , etc... For the notation #Z.X.Y please refer to Section 4.2.7.3.

Table 3: Length of control word

CPRI line bit rate [Mbit/s]	length of word [bit]	control word consisting of BYTES #
614.4	$T=8$	#Z.X.0
1228.8	$T=16$	#Z.X.0, #Z.X.1
2457.6	$T=32$	#Z.X.0, #Z.X.1, #Z.X.2, #Z.X.3

The remaining words ( $W=1\dots15$ ), 15/16 of the basic frame, are dedicated to the U-plane IQ-data transport (IQ data block).

#### 4.2.7.1.2. Transmission Sequence

The control BYTES of one basic frame are always transmitted first. The basic frame structure is shown in Figure 7 to Figure 9 for different CPRI line bit rates.

The bit assignment within a BYTE is aligned with IEEE Std 802.3-2002 [ 1 ], namely bit 7 (MSB) = H to bit 0 (LSB) = A. The physical transmission sequence of the encoded data is defined by the 8B/10B standard according to IEEE Standard 802.3-2002 [ 1 ]. The transmission sequence of the BYTES is indicated on the right hand side of Figure 7 to Figure 9 with one ball representing a BYTE. After 8B/10B encoding the 10bit code-groups (“abcdei fghj”) are transmitted as serial data stream with bit “a” first.

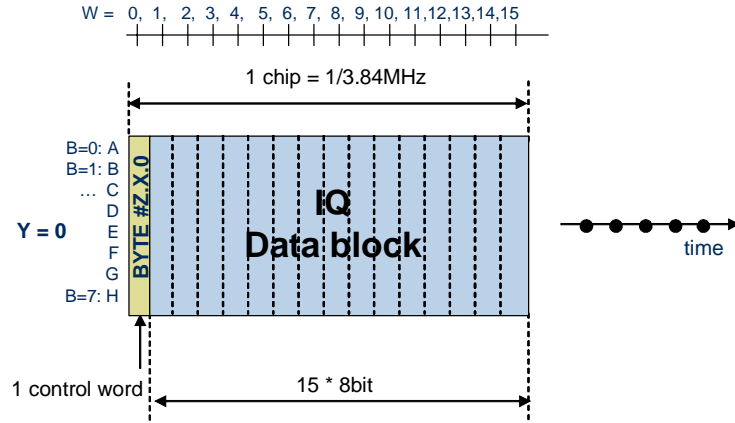


Figure 7: Basic frame structure for 614.4 Mbit/s CPRI line bit rate

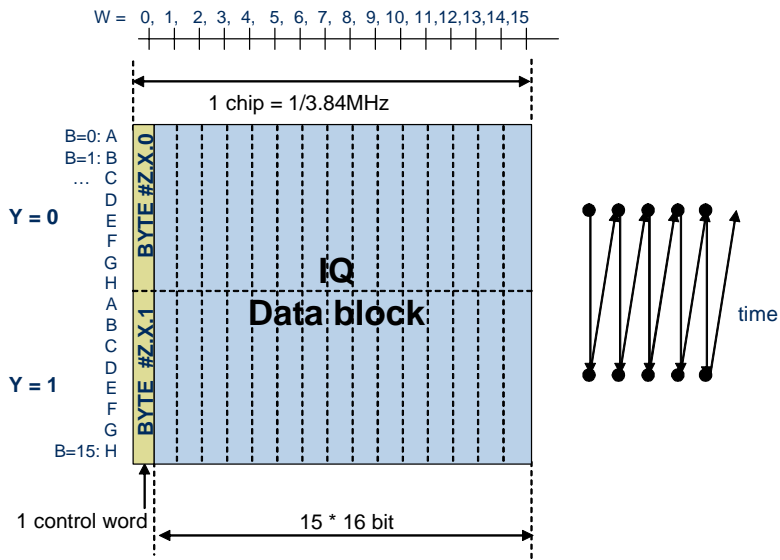


Figure 8: Basic frame structure for 1228.8 Mbit/s CPRI line bit rate

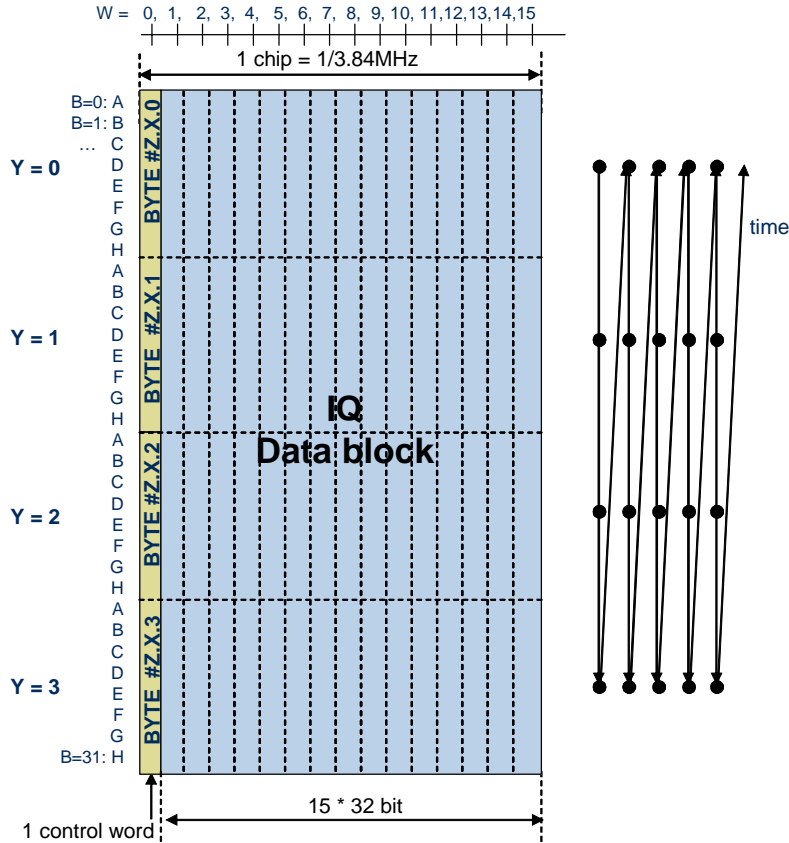


Figure 9: Basic frame structure for 2457.6 Mbit/s CPRI line bit rate

#### 4.2.7.2. Mapping of IQ-data

##### 4.2.7.2.1. IQ Sample Widths

The required sample width of the user-plane IQ-data depends on the application layer. This specification provides a universal mapping scheme in order to implement any of the required sample widths depending on the application layer. The option list for I and Q samples can be found in Table 4. Mixed sample widths within one basic frame are not described in detail but shall also be allowed if required. One IQ sample consists of one I sample and one equal-sized Q sample.

Table 4: Option list for I and Q sample width ranges

Direction of link	Symbol for sample width	Range [bits]
Downlink	M	8, 9, 10, ..., 20
Uplink	M'	4, 5, 6, ..., 10

##### 4.2.7.2.2. Mapping of IQ Samples within one AxC Container

An AxC container is the sub-part of the IQ-data block of the basic frame. It contains  $n$  IQ samples from the same AxC, where  $n$  is the oversampling ratio. IQ sample(s) shall be sent in an AxC container in the following way:

- from LSB ( $I_0, Q_0$ ) to MSB ( $I_{M-1}, Q_{M-1}$ ) or ( $I_{M'-1}, Q_{M'-1}$ ),
- I and Q samples being interleaved,

- in chronological order and
- consecutively without any reserved bits (“r”) in between.

The option list for uplink and downlink oversampling ratios can be found in Table 5.

Table 5: Option list for UL and DL oversampling ratios

	Opt. 1	Opt. 2
DL Oversampling Ratio	1	1
DL Symbols for IQ samples	I,Q	I,Q
UL Oversampling Ratio	2	4
UL Symbols for IQ samples	I, Q, I', Q'	I, Q, I', Q', I'', Q'', I''', Q'''

The IQ sample widths and the oversampling ratios for downlink and uplink shall be decided on application layer per AxC. Figure 10 to Figure 12 show the IQ sample arrangement and the transmission order for uplink and downlink for the described oversampling options.

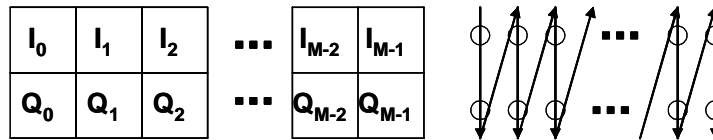


Figure 10: IQ samples within one downlink AxC (oversampling ratio 1)

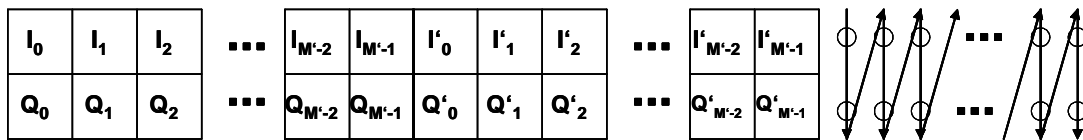


Figure 11: IQ samples within one uplink AxC (oversampling ratio 2)

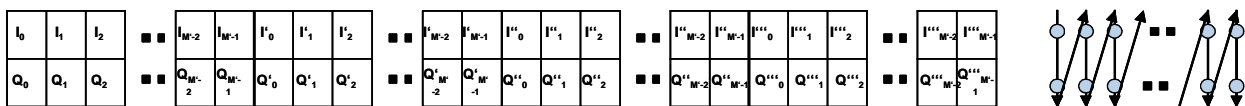


Figure 12: IQ samples within one uplink AxC (oversampling ratio 4)

#### 4.2.7.2.3. Mapping of AxC Container within one Basic Frame

The following mapping rules apply for both directions, uplink and downlink:

- Each AxC container shall be sent as a block.
- No AxC container shall overlap with another AxC container.
- The position of each AxC container in the IQ data block shall be decided by one of the following options:
  - Option 1 (packed position):  
Each AxC container in a basic frame shall be sent consecutively (without any reserved bits in between) and in ascending order of AxC number.
  - Option 2 (flexible position) :

For each AxC container, the application decides at what address (W,B – for W>0) in the IQ data block the first bit of the AxC container shall be positioned. The first bit of an AxC container shall be positioned on an even bit position in the IQ data block (B shall be even).

- The bits not used by AxC containers in the IQ data block in the basic frame shall be treated as reserved bits ("r").

Figure 13 illustrates these mapping rules for both mapping options.

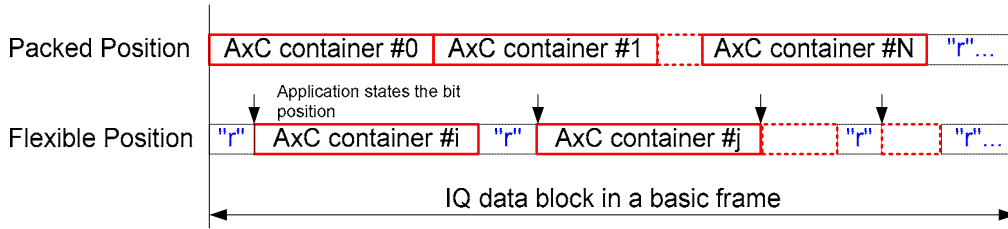


Figure 13: Example of AxC container mapping in the IQ data block

### 4.2.7.3. Hyperframe Structure

The hyperframe structure is hierarchically embedded between the basic frame and the UMTS radio frame as shown in Figure 14.

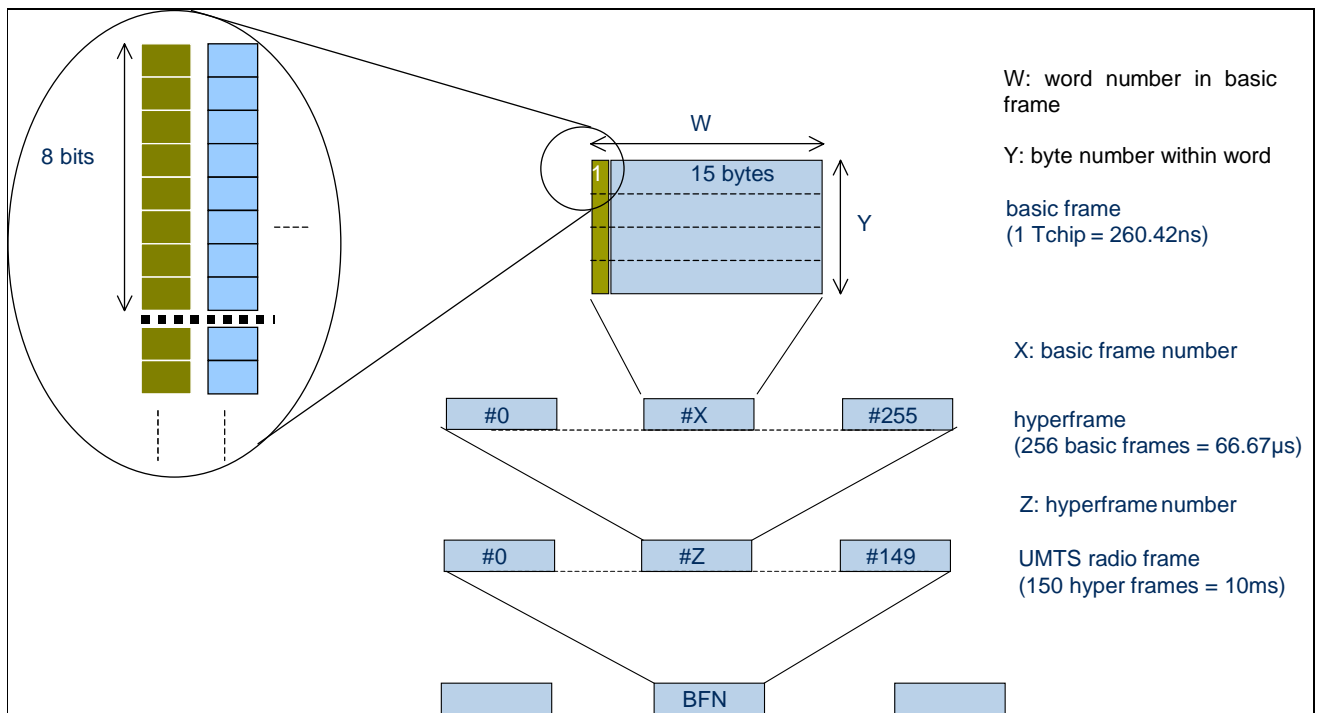


Figure 14: Illustration of the frame hierarchy and notation indices

Z is the hyperframe number, X is the basic frame number within a hyperframe, W is the word number within a basic frame and Y is the byte number within a word. The control word is defined as word with rank W=0. The value ranges of the indices are shown in Table 6:

Table 6: Value ranges of indices

CPRI line bit rate [Mbit/s]	Z	X	W	Y	B
614.4	0, 1, ..., 149	0, 1, ..., 255	0, 1, ..., 15	0	0, 1, ... 7
1228.8				0, 1	0, 1, ... 15
2457.6				0, 1, 2, 3	0, 1, ... 31

4.2.7.4. Subchannel Definition

The 256 control words of a hyperframe are organized into 64 subchannels of 4 control words each. One subchannel contains 4 control words per hyperframe.

The index  $N_s$  of the subchannel ranges from 0 to 63. The index  $X_s$  of a control words within a subchannel has four possible values, namely 0, 1, 2 and 3. The index  $X$  of the control word within a hyperframe is given by  $X = N_s + 64 * X_s$ .

The organization of the control words in subchannels is illustrated in Figure 15 and Figure 16.

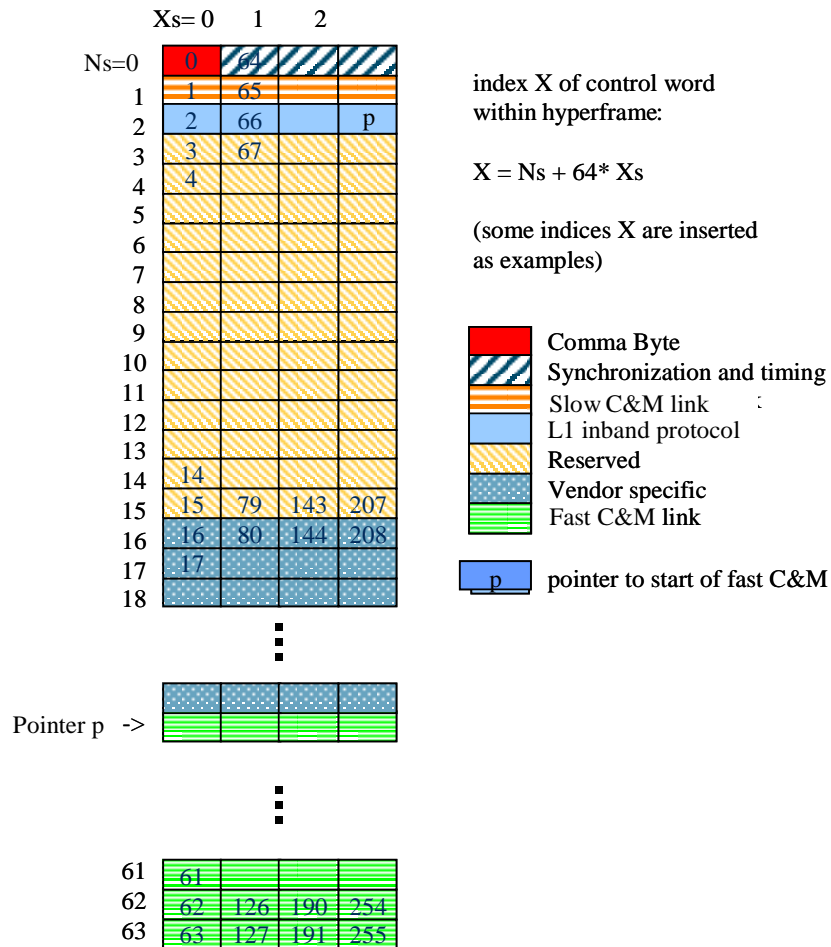


Figure 15: Illustration of subchannels within one hyperframe



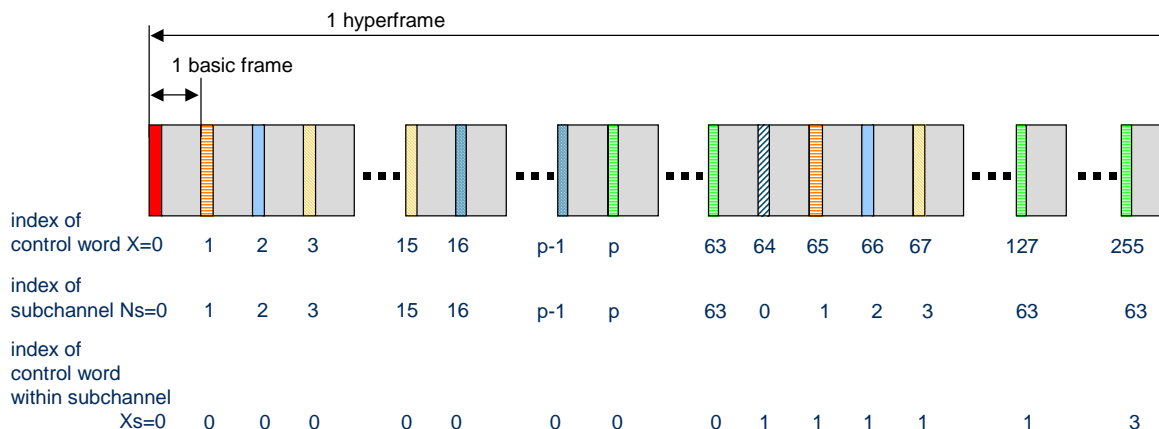


Figure 16: Illustration of control words and subchannels within one hyperframe

Table 7: Implementation of control words within one hyperframe for pointer p &gt; 19

subchannel number Ns	purpose of subchannel	Xs=0	Xs=1	Xs=2	Xs=3
0	sync&timing	sync byte K28.5	HFN	BFN-low	BFN-high
1	slow C&M	slow C&M	slow C&M	slow C&M	slow C&M
2	L1 inband prot.	version	startup	L1-reset-LOS...	pointer p
3	reserved	reserved	reserved	reserved	reserved
...	...	...	...	...	...
15	reserved	reserved	reserved	reserved	reserved
16	vendor specific	vendor specific	vendor specific	vendor specific	vendor specific
...	...	...	...	...	...
p-1	vendor specific	vendor specific	vendor specific	vendor specific	vendor specific
pointer: p	fast C&M	fast C&M	fast C&M	fast C&M	fast C&M
...	...	...	...	...	...
63	fast C&M	fast C&M	fast C&M	fast C&M	fast C&M

For subchannel 0 the content of the control BYTES #Z.X.Y with index  $Y \geq 1$  is reserved ("r"), except for the synchronization control word (Xs=0), where Table 9 applies. For subchannel 1 Table 11 applies. For subchannel 2 the content of the control BYTES #Z.X.Y with index  $Y \geq 1$  is reserved ("r").

#### 4.2.7.5. Synchronization Data

The following control words listed in Table 8 are dedicated to layer 1 synchronization and timing. The support of the control words in Table 8 and Table 9 is mandatory.

Table 8: Control words for layer 1 synchronization and timing

BYTE index	Function	content	comment
Z.0.0	Start of hyperframe	Special code K28.5	
Z.64.0	HFN (Hyperframe number)	HFN=0...149, the first hyperframe in an UMTS radio frame has HFN=0. The exact HFN bit mapping is indicated in Figure 17.	UMTS frame synchronisation, HFN and BFN are described in detail in sections 4.2.8 and 4.2.9.

Z.128.0 and Z.192.0	UMTS NodeB frame  BFN	#Z.128.0 (low byte) and  b3-b0 of #Z.192.0 are BFN  b7-b4 of #Z.192.0 are reserved (all "r"). The exact mapping is described in Figure 18.
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HFN is mapped within #Z.64.0 as defined in Figure 17.

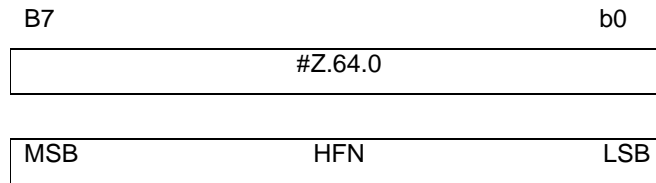


Figure 17: HFN mapping

BFN is mapped within #Z.128.0 and #Z.192.0 as defined in Figure 18. #Z.192.0 b7---b4 are reserved bits.

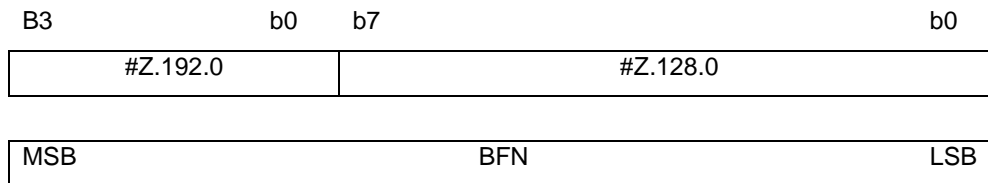


Figure 18: BFN mapping

Table 9: Synchronization control word

CPRI line bit rate [Mbit/s]	Sync. Control Word			
	#Z.0.0	#Z.0.1	#Z.0.2	#Z.0.3
	Sync. Byte	Filling Bytes		
614.4	K28.5(BCh)	NA		
1228.8	K28.5(BCh)	D16.2(50h)	NA	
		D5.6(C5h)		
2457.6	K28.5(BCh)	D16.2(50h)	D16.2(50h)	D16.2(50h)
		D5.6(C5h)		

Remark:

The sequences K28.5+D5.6 and K28.5+D16.2 are defined in the 8B/10B standard as /I1/ and /I2/ ordered\_sets (IDLE1 sequences with opposing disparity and IDLE2 sequences with preserving disparity) and are assumed to be supported by commonly used SERDES devices.

According to table 10, transmitter may send either D16.2 or D5.6 as #Z.X.1 byte. The receiver shall accept both D16.2 and D5.6.

#### 4.2.7.6. L1 Inband Protocol

Reserved bits in this section are marked with "r". This means that a transmitter shall send 0's for bits marked with "r", and the receiver shall not interpret bits marked with "r" (transmit: r = 0, receiver: r = don't care).

The control words listed in Table 10 are dedicated to L1 inband protocol.

Table 10: Control words for L1 inband protocol

BYTE index	function	content	comment
Z.2.0	Protocol version	"0000 0001"	This document refers to protocol version 1
Z.66.0	Startup	<p>"rrrr rCCC"</p> <p>b2-b0 HDLC data rate, DL is master, UL acknowledge):</p> <p>000: no HDLC</p> <p>001: 240kbit/s HDLC</p> <p>010: 480kbit/s HDLC</p> <p>011: 960kbit/s HDLC (not with 614.4 Mbit/s)</p> <p>100: 1920kbit/s HDLC (only with 2457.6Mbit/s)</p> <p>101...111: invalid, reserved; for an overview refer to Table 11</p> <p>b7-b3: reserved (all "r")</p>	Enables the HDLC link to be established
Z.130.0	L1 <u>S</u> DI, <u>R</u> AI, <u>R</u> eset, <u>L</u> OS, <u>L</u> OF	<p>"rrrF LSAR"</p> <p>b0: <u>R</u>eset</p> <p>0: no reset</p> <p>1: reset</p> <p>DL: reset request</p> <p>UL: RE reset acknowledge</p> <p>b1: <u>R</u>AI</p> <p>b2: <u>S</u>DI</p> <p>b3: <u>L</u>OS</p> <p>b4: <u>L</u>OF</p> <p>0: alarm cleared</p> <p>1: alarm set</p> <p>b7-b5: reserved (all "r")</p>	Basic layer 1 functions
Z.194.0	<u>P</u> ointer p	<p>"rrPPPP PP"</p> <p>b5-b0: <u>P</u>ointer to subchannel number, where Ethernet link starts:</p> <p>000000: p=0: no Ethernet</p>	Indicates the subchannel number $N_s$ at which the control words for the Ethernet channel starts within a hyperframe.

		channel 000001 ... 010011: p=1...19 invalid (no Ethernet channel, not possible since other control words would be affected) 010100: ... 111111: p=20...63: valid Ethernet channel, for data rates refer to Table 12  b7-b6: reserved (all "r")	
--	--	--	--

#### 4.2.7.6.1. Reset

Reset of the link is managed through start-up sequence definition (see Section 4.5). Reset of the RE is managed with the Reset bit in #Z.130.0. In UL the RE acknowledges reset notification by setting the reset bit in #Z.130.0. While in reset and if the link is still transmitting, the RE must set the SDI bit.

#### 4.2.7.6.2. Protection of Signalling Bits

Signalling bits shall be protected by filtering over multiple hyperframes. The filtering shall be done by a majority decision of the 5 instances of one signalling bit derived from the 5 most recent hyperframes. The filtering guarantees that 2 consecutive erroneous receptions of instances of one signalling bit do not result in an erroneous interpretation.

This filtering requirement applies to the following signalling bit:

#Z.130.0,b0: "R" (Reset)

The filtering of the other inband protocol bits, i.e., #Z.66.0 (HDLC rate), #Z.194.0 (pointer to Ethernet channel), #Z.130.0 (layer 1 link maintenance) and #Z.2.0 (protocol version) shall be performed by the application layer (see also Section 4.2.10).

#### 4.2.7.7. C&M Plane Data Channels

CPRI supports two different types of C&M channels, which can be selected from the following option list:

- C&M Channel Option 1: Slow C&M Channel based on HDLC
- C&M Channel Option 2: Fast C&M Channel based on Ethernet

##### 4.2.7.7.1. Slow C&M Channel

One option is to use a low rate HDLC channel for C&M data. The data rate shall be according to the 3 LSBs of the "startup information" byte #Z.66.0 (see Table 11). The mapping of control BYTES to HDLC serial data shall be according to what is shown for the different configurations in Figure 19 to Figure 22.

Table 11: Achievable HDLC data rates in kbit/s

CPRI line bit rate [Mbit/s]	#Z.66.0=rrrr r000	#Z.66.0=rrrr r001	#Z.66.0=rrrr r010	#Z.66.0=rrrr r011	#Z.66.0=rrrr r100	#Z.66.0= rrrr r101...rrrr r111
614.4	no HDLC	240	480	invalid	invalid	invalid

1228.8	no HDLC	240	480	960	invalid	invalid
2457.6	no HDLC	240	480	960	1920	invalid
used control words for the HDLC channel and their sequential order	no HDLC	#Z.1.0 #Z.129.0	#Z.1.0 #Z.65.0 #Z.129.0 #Z.193.0	#Z.1.0 #Z.1.1 #Z.65.0 #Z.65.1 #Z.129.0 #Z.129.1 #Z.193.0 #Z.193.1	#Z.1.0 #Z.1.1 #Z.1.2 #Z.1.3 #Z.65.0 #Z.65.1 #Z.65.2 #Z.65.3 #Z.129.0 #Z.129.1 #Z.129.2 #Z.129.3 #Z.193.0 #Z.193.1 #Z.193.2 #Z.193.3	invalid

Remark: In case of an invalid configuration no HDLC shall be used.

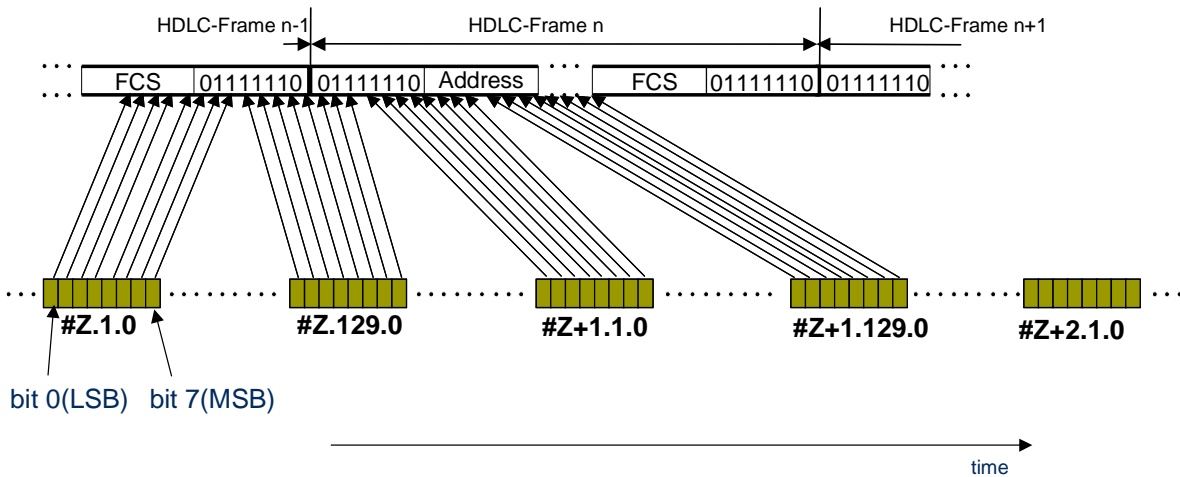


Figure 19: Mapping of control BYTES to HDLC serial data with 240kbit/s

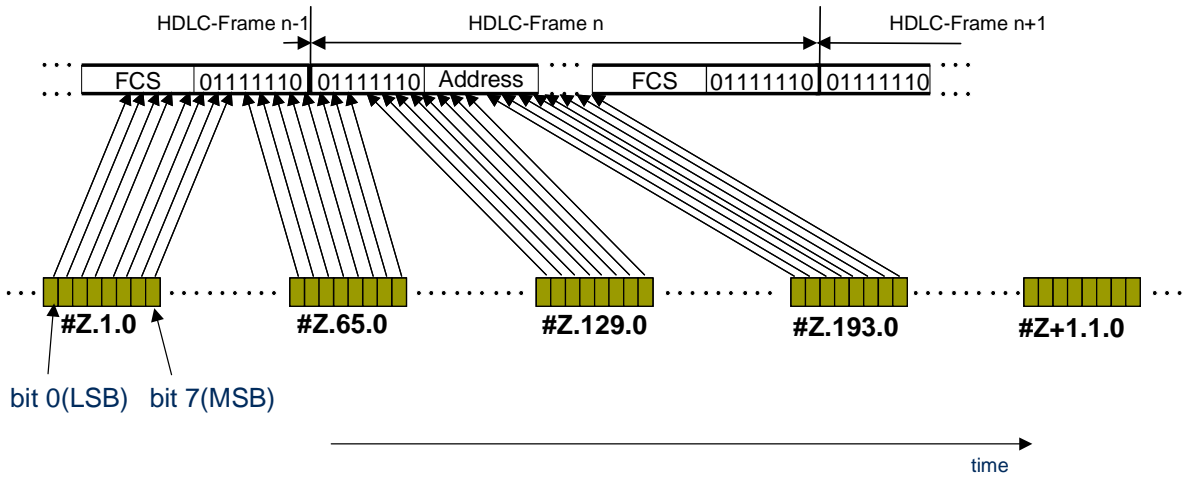


Figure 20: Mapping of control BYTES to HDLC serial data with 480kbit/s

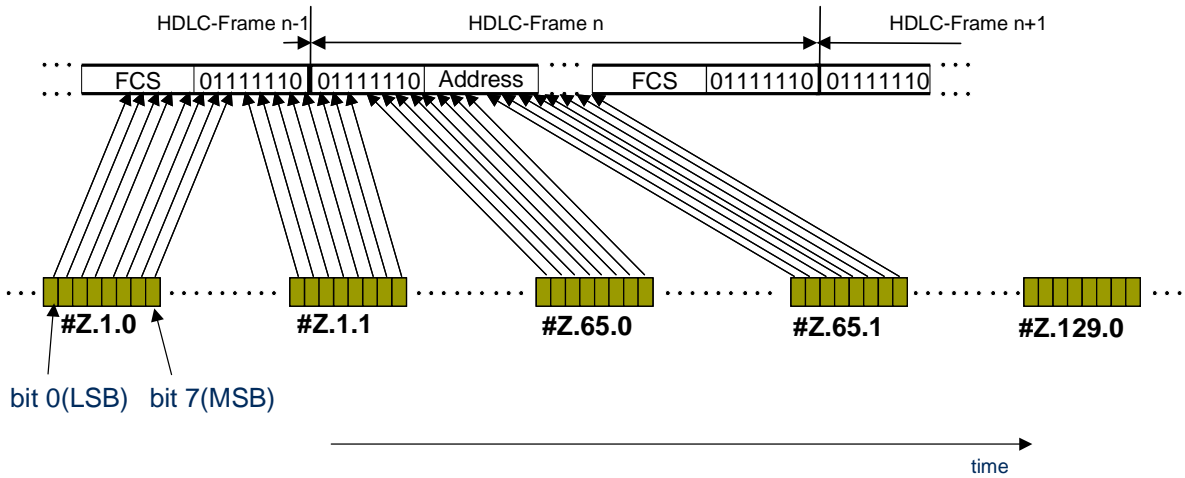


Figure 21: Mapping of control BYTES to HDLC serial data with 960kbit/s

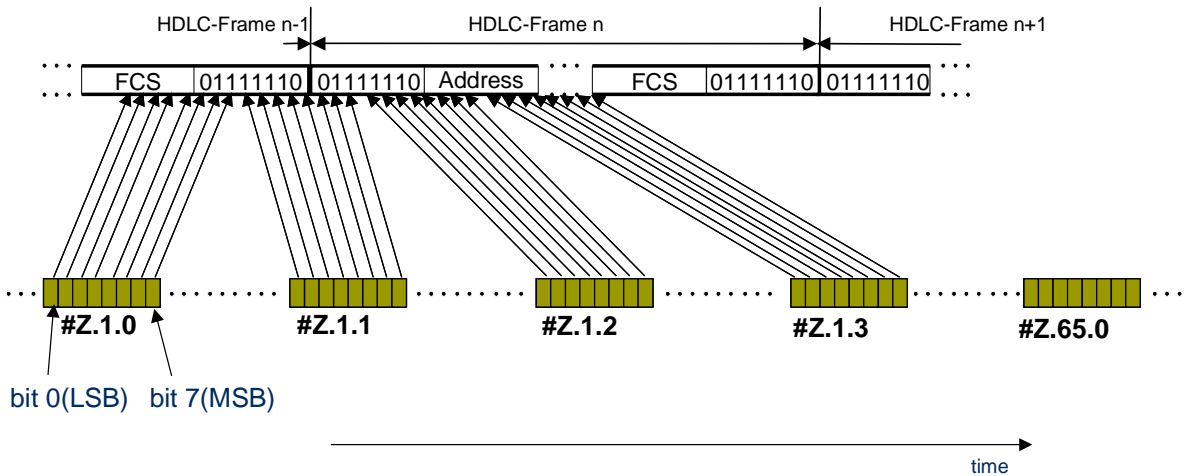


Figure 22: Mapping of control BYTES to HDLC serial data with 1920kbit/s

#### 4.2.7.7.2. Fast C&M Channel

Another option is to use a high data rate Ethernet Channel which can flexibly be configured by the pointer in control byte #Z.194.0. The mapping of the Ethernet data follows the same principle as the HDLC channel (no BYTE alignment, LSB first).

The Ethernet data rate shall be configured with the pointer in control byte #Z.194.0. In contrast to the HDLC link, the full control words shall always be used for the Ethernet channel. The achievable Ethernet data rates are shown in Table 12.

Table 12: Achievable Ethernet data rates

CPRI line bit rate [Mbit/s]	length of control word [bit]	control word consisting of BYTES #	minimum Ethernet data rate [Mbit/s] (#Z.194.0=rr111111)	maximum Ethernet data rate [Mbit/s] (#Z.194.0=rr010100)
614.4	8	#Z.X.0	0.48	21.12
1228.8	16	#Z.X.0, #Z.X.1	0.96	42.24
2457.6	32	#Z.X.0, #Z.X.1, #Z.X.2, #Z.X.3	1.92	84.48

Packet detection, start and termination shall be based on SSD and ESD coding sequence as shown in Figure 23.

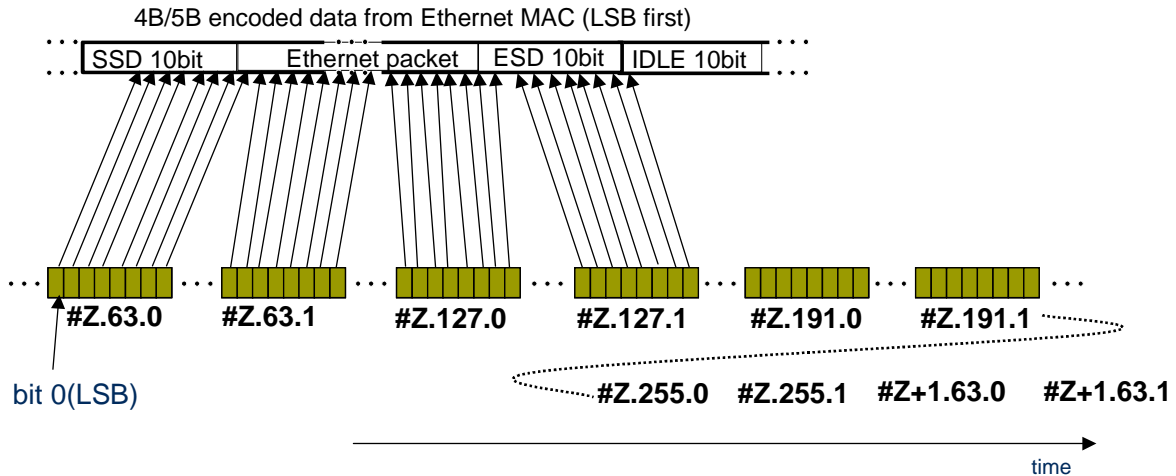


Figure 23: Example showing the mapping of control BYTES to Ethernet channel at 1228.8Mbit/s CPRI line bit rate and pointer BYTE #Z.194.0=rr111111

#### 4.2.7.7.3. Minimum C&M Channel Support

The use of either HDLC or Ethernet is optional. It is mandatory for each REC or RE to support at least one non-zero C&M channel rate on at least one link.

#### 4.2.7.7.4. Links for Capacity Expansion / Passive Link

Links for capacity expansion do not need to support any C&M channel. A link for capacity expansion or a passive link may be requested by the REC indicating #Z.66.0 = rrrr r000 and #Z.194.0 = rr00 0000 (r = reserved, transmit 0, receiver don't care) in downlink.

#### 4.2.7.8. Future Protocol Extensions

52 control words of one hyperframe are reserved for future interface protocol extensions. Reserved words are completely filled with reserved bits (reserved bits are marked with "r"). This means that a transmitter shall

send 0's for bits marked with "r", and the receiver shall not interpret bits marked with "r". (transmit: r = 0, receiver: r = don't care).

#### 4.2.7.9. Vendor Specific Data

Depending on the usage of the fast C&M channel up to 192 control words (in subchannels 16 to 63) of one hyperframe are available for vendor specific data. A minimum of 16 control words (in subchannels 16 to 19) per hyperframe are reserved for vendor specific data.

#### 4.2.8. Synchronisation and Timing

The RE shall use the incoming bit clock as the source for the radio transmission and the uplink bit clock. The time information is transferred from the REC to the RE through the information described 4.2.7.5. The UMTS frame delimitation is provided by the K28.5 symbol of the hyperframe number #0.

#### 4.2.9. Delay Calibration

The interface provides the basic mechanism to enable calibrating the delay between REC and RE. More specifically, the reference points for delay calibration and the timing relation between input and output signals at RE are defined.

##### 4.2.9.1. Definition of Reference Points for Delay Calibration

The reference points for delay calibration are the input and the output points of the equipment, i.e. connectors of REC and RE as shown in Figure 24. Reference Points #1-4 correspond to the output point of REC (R1), the input point of RE (R2), the output point of RE (R3) and the input point of REC (R4) respectively. The antenna is shown as "Ra" for reference.

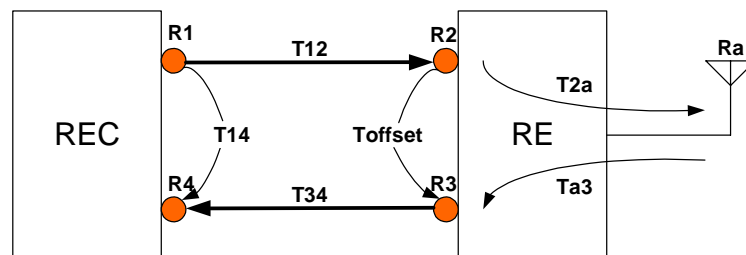


Figure 24: Definition of reference points for delay calibration

##### 4.2.9.2. Relation between Downlink and Uplink Frame Timing

Figure 25 shows the relation between downlink and uplink frame timing.

- **T12** is the delay of downlink signal from the output point of REC (**R1**) to the input point of RE (**R2**).
- **T34** is the delay of uplink signal from the output point of RE (**R3**) to the input point of REC (**R4**).
- **Toffset** is the frame offset between the input signal at **R2** and the output signal at **R3**.
- **T14** is the frame timing difference between the output signal at **R1** and the input signal at **R4**.

RE shall determine the frame timing of its output signal (uplink) to be the fixed offset (**Toffset**) relative to the frame timing of its input signal (downlink). This fixed offset (**Toffset**) is an arbitrary value, which shall be greater than or equal to 0 and less than  $256 T_c$ . In case the system shall fulfil R-21 (delay calibration) then **Toffset** accuracy shall be lower than  $T_c/32$ . Different REs may use different values for **Toffset**. REC shall know the value of **Toffset** of each RE in advance (e.g. pre-defined value or RE informs REC by higher layer message). In addition, the downlink BFN and HFN from REC to RE shall be given back in uplink from the RE to the REC. In case of an uplink signalled LOS, LOF, RAI or SDI the REC shall treat the uplink BFN and HFN as invalid.



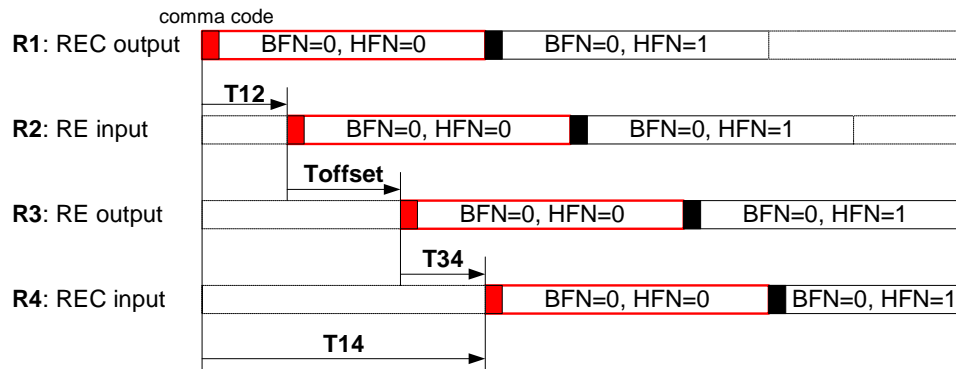


Figure 25: Relation between downlink and uplink frame timing

## 4.2.10. Link Maintenance of Physical Layer

### 4.2.10.1. Definition

Four Layer 1 alarms are defined

- Loss of Signal (LOS)
- Loss of Frame (LOF)
- Remote Alarm Indication (RAI)
- SAP Defect Indication (SDI)

For each of these alarms a bit is allocated in the CPRI hyperframe to remotely inform the far end equipment of the occurrence of the alarm.

On detection of the alarm at near end the inband bit is “immediately” –up to the performance of the device– set and forwarded on CPRI to the far end. When the alarm is cleared the inband bit is reset.

Notice that to be able to receive and decode such information, the remote equipment must be at least in state C of start-up (for state definition, see Section 4.5).

Local actions are undertaken at both near and far end when failure is detected.

Failure is:

- defined when the alarm persists.
- set after time filtering of the alarm.
- cleared after time filtering of the alarm.

The timers for near and far end filtering are defined by the application layer.

### 4.2.10.2. Loss of Signal (LOS)

#### 4.2.10.2.1. Detection

The CPRI definition of LOS shall be when at least 16 8B/10B violations occur among a whole hyperframe.

For optical mode of CPRI, detection of LOS may also be achieved by detecting light power below a dedicated threshold. Detection speed shall within one Hyperframe duration.

#### 4.2.10.2.2. Cease

The alarm shall be cleared when a whole hyperframe is received without code violation.

4.2.10.2.3. Inband Bit

The inband bit that transport this information is Z.130.0 b3

4.2.10.2.4. Local Action

**RE**

Upon detecting such a failure, the RE shall go into state B of the start-up sequence (see Section 4.5). In addition it is HIGHLY recommended that appropriate actions be performed to prevent from emitting on the radio interface.

**REC**

On detecting such a failure, the REC shall go into state B of the start-up sequence.

4.2.10.2.5. Remote Action

**RE**

When detecting such a failure, based on the received information, the RE shall go into state B of the start-up sequence.

In addition it is HIGHLY recommended that appropriate actions be performed to prevent from emitting on the radio interface.

**REC**

When detecting such a failure, based on the received information, the REC shall go into state B of start-up sequence.

4.2.10.3. Loss of Frame (LOF)

4.2.10.3.1. Detection

This alarm shall be detected if the hyperframe alignment cannot be achieved or is lost as defined in Figure 26.

Number of XACQ state and XSYNC state is restricted to acquisition time limitation. Figure 26 shows 2 XACQ and 3 SYNC states as an example.

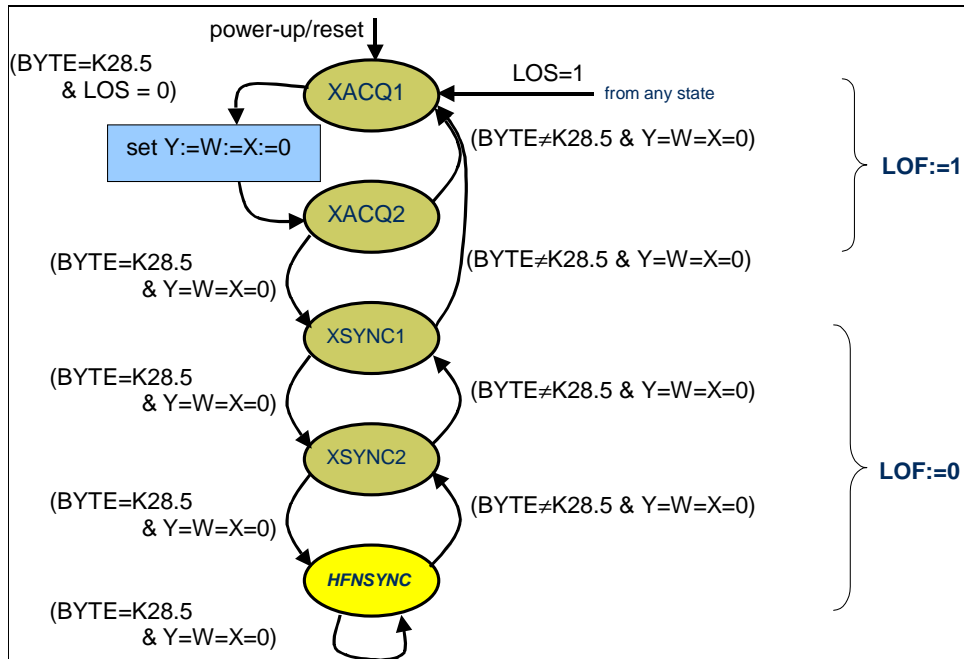


Figure 26: Example for LOF and HFNSYNC detection

#### 4.2.10.3.2. Cease

This alarm shall be cleared if the hyperframe alignment is achieved as defined in Figure 26.

#### 4.2.10.3.3. Inband Bit

The inband bit that transports this information is Z.130.0 b4

#### 4.2.10.3.4. Local Action

##### **RE**

When detecting such a failure the RE shall go in state B of start-up sequence.

In addition it is HIGHLY recommended that appropriate actions be performed to prevent emission on the radio interface.

##### **REC**

When detecting such a failure, based on the received information, the REC shall go in state B of start-up sequence.

#### 4.2.10.3.5. Remote Action

##### **RE**

When detecting such a failure, based on the received information, the RE shall go in state B of start-up sequence.

In addition it is HIGHLY recommended that appropriate actions be performed to prevent emission on the radio interface.

##### **REC**

When detecting such a failure, based on the received information, the REC shall go in state B of start-up sequence.

#### 4.2.10.4. Remote Alarm Indication

##### 4.2.10.4.1. Detection

Any errors, including LOS and LOF, that are linked to CPRI transceiver shall be indicated by the RAI information.

##### 4.2.10.4.2. Cease

When no errors, including LOS and LOF, are linked to the CPRI transceiver, the RAI shall be cleared.

##### 4.2.10.4.3. Inband Bit

The Remote Alarm Indication bit is used to transport this information: Z.130.0 b1

##### 4.2.10.4.4. Local Action

##### **RE**

Out of scope of CPRI.

##### **REC**

Out of scope of CPRI.

##### 4.2.10.4.5. Remote Action

##### **RE**

When detecting such a failure, based on the received information, the RE shall go in state B of start-up sequence.

In addition it is HIGHLY recommended that appropriate actions be performed to prevent from emitting on the radio interface.

#### **REC**

When detecting such a failure, based on the received information, the REC shall go in state B of start-up sequence.

#### 4.2.10.5. SAP Defect Indication

A link is said to be in “alarm” when the near end explicitly informs the far end equipment that the link shall not be used for any of the Service Access Points.

Notice in this case the CPRI link is fully available and decoded by the far end receiver.

##### 4.2.10.5.1. Detection

The detection procedure is outside the scope of CPRI. This is fully application dependant.

##### 4.2.10.5.2. Cease

The alarm reset procedure is outside the scope of CPRI. This is fully application dependant.

##### 4.2.10.5.3. Inband Bit

The SAP Defect Indication Signal bit is used to transport this information: Z.130.0 b2

##### 4.2.10.5.4. Local Action

#### **RE**

N/A

#### **REC**

N/A

##### 4.2.10.5.5. Remote Action

#### **RE**

The RE shall not use this link anymore for any of the CPRI Service Access Points: IQ, Sync or C&M. In addition it is HIGHLY recommended that appropriate actions be performed to prevent from emitting on the radio interface.

#### **REC**

The REC shall not use this link anymore for any of the CPRI Service Access Points: IQ, Sync or C&M.

### 4.3. Data Link Layer (Layer 2) Specification for Slow C&M Channel

CPRI slow C&M Data Link Layer shall follow the HDLC standard ISO/IEC 13239:2002 (E) [ 10 ] using the bit oriented scheme.

#### 4.3.1. Layer 2 Framing

HDLC data frames and Layer 2 procedures shall follow [ 10 ]. In addition the CPRI Layer 2 for the slow C&M link shall fulfil the following additions:

- **Information Field Length**  
HDLC information field length in HDLC frames shall support any number of octets.
- **Bit Transmission Order of the Information Part**  
HDLC Information field bit transmission order in HDLC frames shall be least significant bit (LSB) first.

- **Address field**  
HDLC frames shall use a single octet address field and all 256 combinations shall be available. Extended address field shall not be used in HDLC data frames.
- **Frame Format**  
HDLC data frames shall follow the basic frame format according to ISO/IEC 13239:2002 (E) [ 10 ], chapter 4.1.1.<sup>1</sup>

### 4.3.2. Media Access Control/Data Mapping

Media Access Control/Data Mapping shall follow chapter 4.2.7.7.1 of this specification.

### 4.3.3. Flow Control

CPRI slow C&M link flow control shall follow HDLC standard ISO/IEC 13239:2002 (E) [ 10 ]. In addition CPRI Layer 2 for the slow C&M link shall fulfil the following additions:

- **Flags**  
HDLC frames shall always start and end with the flag sequence. A single flag must not be used as both the closing flag for one frame and the opening flag for the next frame.
- **Inter-frame time fill**  
'Inter-frame time fill' between HDLC frames shall be accomplished by contiguous flags.

### 4.3.4. Control Data Protection/ Retransmission Mechanism

CPRI slow C&M link data protection shall follow HDLC standard ISO/IEC 13239:2002 (E) [ 10 ]. In addition CPRI Layer 2 for the slow C&M link shall fulfil the following addition:

- **Frame Check Sequence (FCS)**  
CPRI slow C&M link shall support a FCS of length 16 bit as defined in ISO/IEC 13239:2002 (E) [ 10 ].

Retransmission mechanisms shall be accomplished by higher layer signalling.

## 4.4. Data Link Layer (Layer 2) Specification for Fast C&M Channel

CPRI C&M Fast Data Link Layer shall follow the Ethernet standard as specified in IEEE std 802.3-2002 [ 1 ].

### 4.4.1. Layer 2 Framing

Data mapping in Layer 2 shall follow section "3. Media access control frame structure" of IEEE std 802.3-2002 [ 1 ].

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<sup>1</sup> FCS transmission order in HDLC frames shall be most significant bit (MSB) first as defined in the HDLC standard.

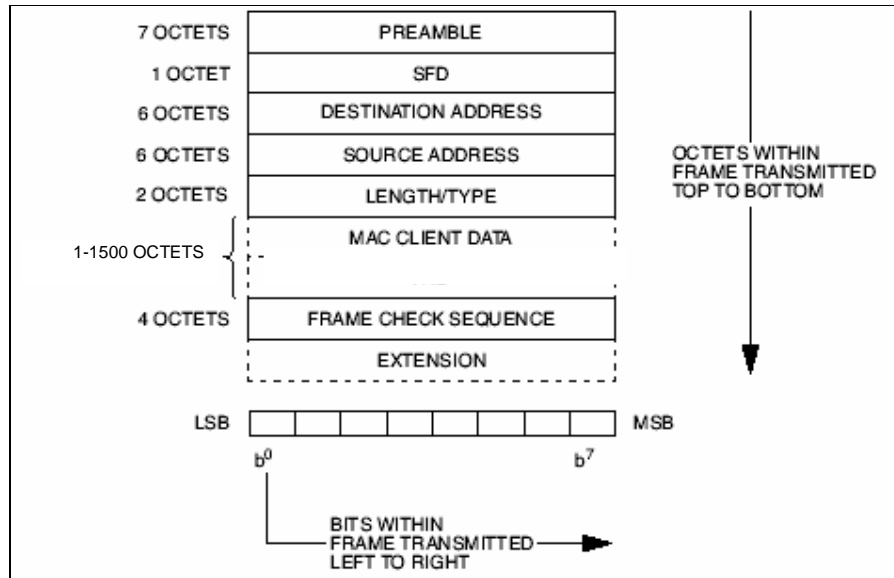


Figure 27: Layer 2 Framing

**Specific CPRI requirements:****Minimum Ethernet frame length and padding:**

Due to the specific CPRI framing, no minimum frame length makes any sense for CPRI application. CPRI does not specify any minimum frame size and does not require frame padding.

The MAC client Data + PAD field length shall range from 1 to 1500 octets.

**Extension field:**

The extension field must not be used within CPRI.

**4.4.2. Media Access Control/Data Mapping**

Layer 2 data mapping in the CPRI frame is performed according to section “4.2.7.7.2 Fast C&M channel” of this specification.

In addition the Ethernet frame shall be controlled and mapped through usage of section “24.2 Physical Coding SubLayer (PCS)” of IEEE Std 802.3-2002 [ 1 ] concerning 100BASE-X.

PCS supports 4 main features that are not all used by CPRI (see Table 13):

Table 13: PCS features used by CPRI

Feature	CPRI support
Encoding/Decoding	Fully supported by CPRI
Carrier sense detection and collision detection	<i>Irrelevant to CPRI</i>
Serialization/deserialization	<i>Irrelevant to CPRI</i>
Mapping of transmit, receive, carrier sense and collision detection	<i>Irrelevant to CPRI</i>

Table 24-4 in “24. Physical Coding SubLayer (PCS) and Physical Medium Attachment (PMA) sublayer, type 100BASE-X” of IEEE Std 802.3-2002 [ 1 ] is modified as shown in Figure 28:

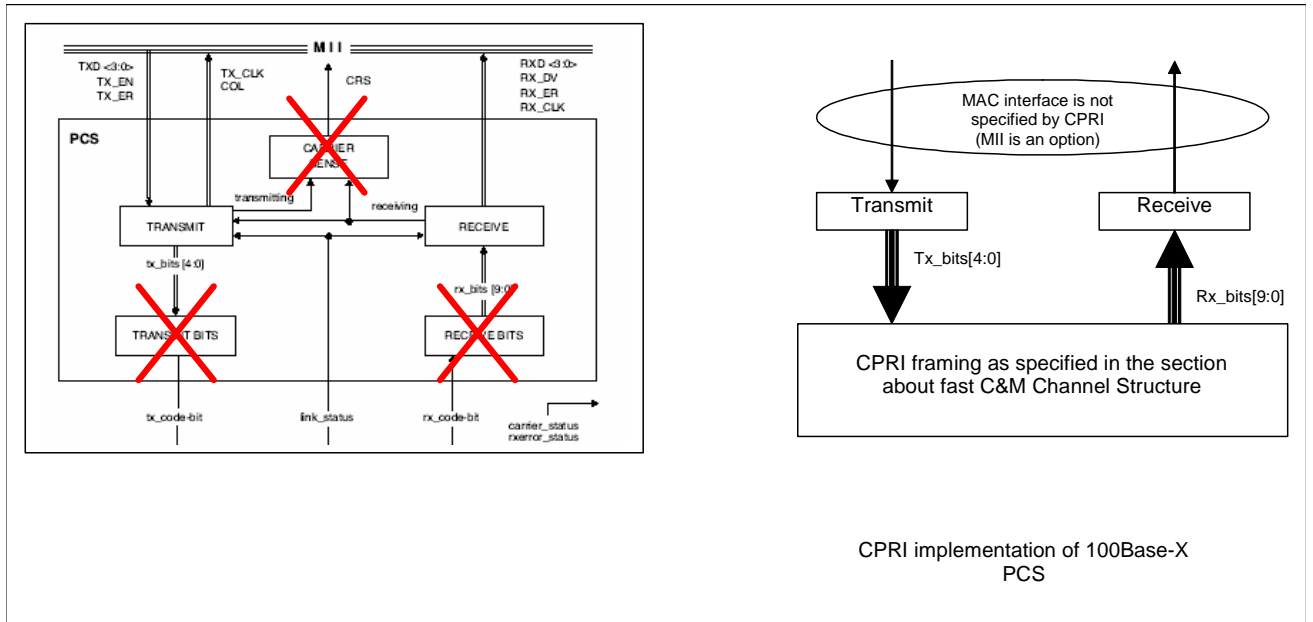


Figure 28: CPRI implementation of 100BASE-X PCS

The Ethernet MAC frame shall be encoded using the 4B/5B code of 100BASE-X PCS (Physical Coding Sublayer) as specified in section 24.2 of IEEE std 802.3-2002 [ 1 ].

The 4B/5B code list shall be according table 24.1 of IEEE std 802.3-2002 [ 1 ] (see below).

Table 14: 4B/5B code list (modified Table 24.1 of IEEE 802.3-2002 [ 1 ])

	PCS code-group [4:0] 4 3 2 1 0	Name	MAC Client Data nibble	Interpretation
D A T A	1 1 1 1 0	0	0 0 0 0	Data 0
	0 1 0 0 1	1	0 0 0 1	Data 1
	1 0 1 0 0	2	0 0 1 0	Data 2
	1 0 1 0 1	3	0 0 1 1	Data 3
	0 1 0 1 0	4	0 1 0 0	Data 4
	0 1 0 1 1	5	0 1 0 1	Data 5
	0 1 1 1 0	6	0 1 1 0	Data 6
	0 1 1 1 1	7	0 1 1 1	Data 7
	1 0 0 1 0	8	1 0 0 0	Data 8
	1 0 0 1 1	9	1 0 0 1	Data 9
	1 0 1 1 0	A	1 0 1 0	Data A
	1 0 1 1 1	B	1 0 1 1	Data B
	1 1 0 1 0	C	1 1 0 0	Data C
	1 1 0 1 1	D	1 1 0 1	Data D
	1 1 1 0 0	E	1 1 1 0	Data E
	1 1 1 0 1	F	1 1 1 1	Data F
	1 1 1 1 1	I	undefined	IDLE; used as inter-stream fill code
C O N T R O L	1 1 0 0 0	J	0 1 0 1	Start-of-Stream Delimiter, Part 1 of 2; always used in pairs with K
	1 0 0 0 1	K	0 1 0 1	Start-of-Stream Delimiter, Part 2 of 2; always used in pairs with J
	0 1 1 0 1	T	undefined	End-of-Stream Delimiter, Part 1 of 2; always used in pairs with R
	0 0 1 1 1	R	undefined	End-of-Stream Delimiter, Part 2 of 2; always used in pairs with T
I N V A L I D	0 0 1 0 0	H	Undefined	Transmit Error; used to force signaling errors
	0 0 0 0 0	V	Undefined	Invalid code
	0 0 0 0 1	V	Undefined	Invalid code
	0 0 0 1 0	V	Undefined	Invalid code
	0 0 0 1 1	V	Undefined	Invalid code
	0 0 1 0 1	V	Undefined	Invalid code
	0 0 1 1 0	V	Undefined	Invalid code
	0 1 0 0 0	V	Undefined	Invalid code
	0 1 1 0 0	V	Undefined	Invalid code
	1 0 0 0 0	V	Undefined	Invalid code
	1 1 0 0 1	V	Undefined	Invalid code

The Ethernet frame shall be delineated by the PCS function as shown in Figure 29:



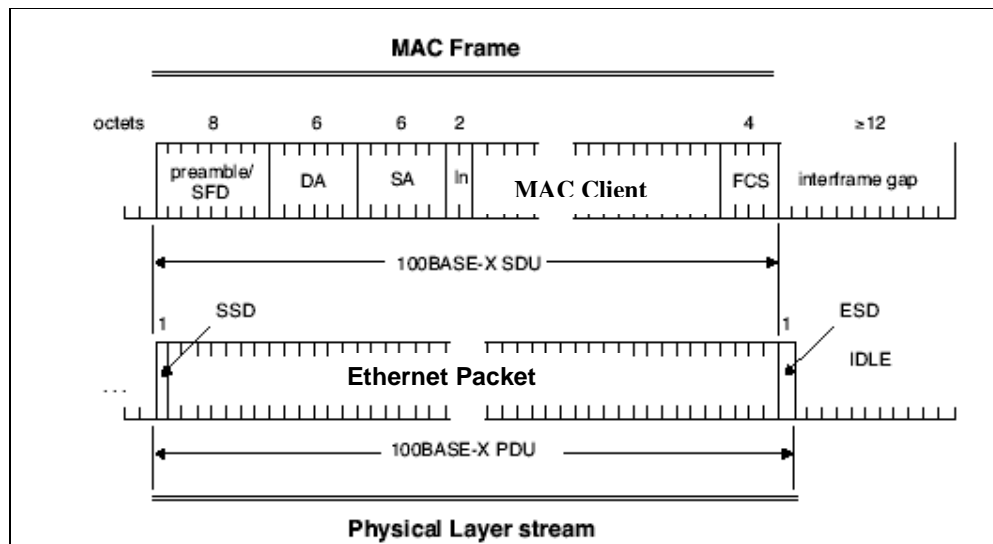


Figure 29: Physical Layer Stream of 100BASE-X

### 4.4.3. Flow Control

No flow control is provided for the fast C&M channel.

### 4.4.4. Control Data Protection/ Retransmission Mechanism

Data protection shall follow section “3.2.8. Frame Check Sequence (FCS) field” of IEEE std 802.3-2002 [ 1 ]. No retransmission mechanism is specified for Fast C&M channel Layer 2.

## 4.5. Start-up Sequence

### 4.5.1. General

The startup procedure accomplishes two main things:

- Synchronization of layer 1: byte alignment and hyper frame alignment
- Alignment of capabilities of the REC and RE: line bit rate, protocol, C&M link speed, C&M protocol, vendor specific signalling

Since there is no mandatory line bit rate or C&M link speed the REC and RE must, during the start-up procedure, try different configurations until a common match is detected. The common match does not have to be optimal – it shall be considered as just a first contact where capabilities can be exchanged for a proper configuration to be used in the following communication.

For all states, it is mandatory to always transmit information consistent with the protocol indicated in Z.2.0 on all control words on sub-channel 1 and sub-channels 3 to 15.

When changing the line bit rate of the transmitted CPRI, the interruption of transmission shall be less than 0.1s. When changing the line bit rate of the received CPRI, the interruption of reception shall be less than 0.1s. The time to reach HFNSYNC for the receiving unit shall be less than 0.2 s, given the precondition that the far-end transmitter is on, they use the same line bit rate and no bit errors occur.

In the negotiation steps in state C and D the REC and RE shall sample and evaluate the received protocol version and C&M bit rates at a rate of at least every 0.1 s. The transmitted protocol version and C&M bit rates shall be updated within 0.2 s after the evaluation.

### 4.5.2. Layer 1 Start-up Timer

The start-up procedure may be endless due to two reasons:

- Fault in one of the units
- No common layer 1 protocol or C&M link speed or C&M type.

The supervision may be done per state and per cause, but the start-up procedure also specifies a generic start-up timer which shall be set upon entry of the start-up procedure and shall be cleared when the C&M link is established.

If the timer expires the start-up procedure shall be restarted.

The “layer 1 start-up timer” is activated in transitions 2, 5, 8, 12, 13, 15.

The “layer 1 start-up timer” is cleared in transitions 6, 9, 10, 11, 14 and in state E when the higher layer C&M connection is established.

If the “layer 1 start-up timer” expires, transition 16 shall take place and state B is entered, possibly modifying the available set of line bit rates and protocols.

The “layer 1 start-up timer” expiration time is vendor specific.

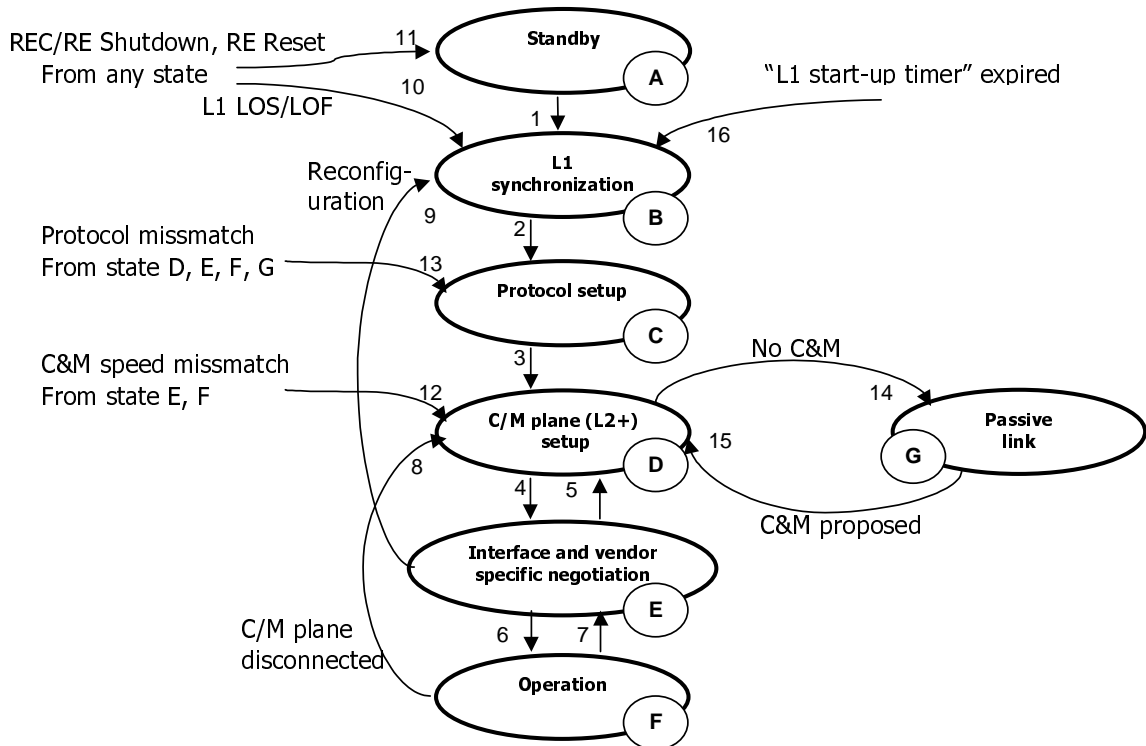


Figure 30: Startup states and transitions

### 4.5.3. State Description

#### 4.5.3.1. State A – Standby

Prerequisites:

None

Description:

Waiting to be configured to start up CPRI. No transmission or reception of CPRI. The operator may configure a suitable startup configuration (line bit rate, C&M link characteristics). The REC and RE may also have knowledge about a previous successful configuration.

### 4.5.3.2. State B – L1 Synchronization and Rate Negotiation

Prerequisites:

The set of available line bit rate, protocol versions and C&M plane characteristics are known. This may be the complete set of the unit or a subset based on operator configuration or previous negotiation between the units (e.g. from state E).

Description:

During this state, the line bit rate of the interface is determined and both REC and RE reaches layer 1 synchronization up to state HFNSYNC.

Interpreted control words:

Z.0.0, Z.64.0

REC actions:

The REC starts to transmit the CPRI at the highest available line bit rate directly when entering the state, and also start to attempt to receive a CPRI at the same line bit rate. If the REC does not reach synchronization state HFNSYNC it shall select another line bit rate from CPRI transmission after time T1 from entering the state, given that another line bit rate is available. T1 is 0.9-1.1 s. Each following T1 interval, a new line bit rate for reception and transmission shall be selected, given that another line bit rate is available. The line bit rates shall be selected from the available set in a round robin fashion, i.e. first highest, the second highest, ..., the slowest, and then restarting from the highest line bit rate.

While in this state, the REC shall set the protocol version in Z.2.0 to its highest available protocol version, and the C&M bit rates in Z.66.0 and Z.194.0 to its highest available C&M bit rates, for the transmitted line bit rate.

RE actions:

The RE shall start attempting to receive CPRI at the highest available line bit rate directly when entering the state. If the RE does not reach synchronization state HFNSYNC it shall select another line bit rate for CPRI reception after T1' from entering the state, given that another line bit rate is available. T1' is 3.9-4.1s. Each following T1' interval, a new reception line bit rate shall be selected for reception, given that another line bit rate is available. The line bit rates shall be selected from the available set in a round robin fashion, i.e. first highest, the second highest, ..., the slowest, and then restarting from the highest line bit rate.

When entering this state, the RE shall turn off its CPRI transmitter. When the RE reach synchronization state HFNSYNC, it shall start transmit CPRI on the same line bit rate.

While in this state, the RE shall set the protocol version in Z.2.0 according to the rule in state C, below, or to the highest available protocol version, for the transmitted bit rate. While in this state, the RE shall set the C&M bit rates in Z.66.0 and Z.194.0 according to the rule in state D, or to the highest available C&M bit rate, for the transmitted line bit rate.

Comments:

While in this state, no timer to detect hanging is provided by the startup procedure. Such a hanging will occur only in case of HW fault and that is detected by vendor specific means.

### 4.5.3.3. State C – Protocol Setup

Prerequisites:

Layer 1 is synchronized, i.e., up- and downlink hyper frame structures are aligned.

Description:

During this state, a common protocol version of CPRI is determined.

Interpreted control words:

Z.0.0, Z.64.0, Z.2.0

REC actions:

The REC shall select its highest available protocol version when entering this state. The protocol version shall be stated in Z.2.0. When the REC receives a valid or an updated protocol version from the RE,

- If the currently received protocol version is equal to the current protocol version sent by REC, the protocol setup is achieved
- If the currently received protocol version differs from the current protocol version sent by the REC, it shall reselect the protocol version. The new protocol version shall be selected according to the rule:

New REC protocol version = highest available protocol version which is less or equal to received RE protocol version (received in Z.2.0)

Error case: If no such protocol exists:

New REC protocol version = lowest available protocol version

Note that the reselection may choose the already transmitted protocol version. The new selected protocol version shall be stated in Z.2.0. If the currently received protocol version is equal to the new protocol version sent by REC, the protocol setup is achieved.

#### RE actions:

The RE shall decode the received protocol version by looking at Z.2.0. When the RE receives a valid or an updated protocol version from the REC,

- If the currently received protocol version is equal to the current protocol version sent by RE, the protocol setup is achieved
- If the currently received protocol version differs from the current protocol version sent by the RE, the RE shall reselect the protocol version. The new proposed protocol version shall be selected according to the rule:

New RE protocol version = highest available protocol version which is less or equal to received REC protocol version (received in Z.2.0)

Error case: If no such protocol exists:

New RE protocol version = lowest available protocol version

Note that the reselection may choose the already transmitted protocol version. The new selected protocol version shall be stated in Z.2.0. If the currently received protocol version is equal to the new protocol version sent by RE, the protocol setup is achieved.

#### Comments:

If the REC does not receive a new protocol version before the layer 1 start-up timer expires, it can assume that there are no common protocol versions. Such a detection can be made faster but then the application must take into account the case where the RE enters the state after the REC. Layer 1 control bits can start to be interpreted but since they require error protection filtering (majority decision) the interpretation is not available until in next state, D.

### 4.5.3.4. State D – C&M Plane (L2+) Setup

#### Prerequisites:

Layer 1 is synchronized and the protocol is agreed on.

#### Description:

During this state, a common C&M link bit rate is determined.

#### Interpreted control words:

All

#### REC actions:

The REC shall select its highest available C&M link bit rate when entering this state: Highest available HDLC bit rate and highest available Ethernet bit rate. The bit rates shall be stated in Z.66.0 and Z.194.0. When the REC receives a valid or an updated bit rate in either Z.66.0 or Z.194.0 from the RE,

- If at least one of the currently received bit rate is equal to the corresponding bit rate sent by REC, the C&M plane setup is achieved
- If both currently received bit rates differ from the current bit rates sent by the REC, the REC shall reselect the C&M link bit rate in Z.66.0 and in Z.194.0. Each new bit rate shall be selected according to the rule:

New REC bit rate = highest available bit rate which is less or equal to received RE bit rate (received in Z.66.0 or Z.194.0)

Error case: The resulting bit rate according to the rule is “no link”, i.e. 0 bit rate:

New REC bit rate = lowest available bit rate

Note that the reselection may choose the already transmitted C&M bit rates. The new selected bit rates shall be stated in Z.66.0 and Z.194.0. If at least one of the currently received bit rate is equal to the corresponding new bit rate sent by REC, the C&M plane setup is achieved.

The REC shall check that Z.2.0 is equal in uplink and downlink. If it is not equal it shall enter state C.

RE actions:

The RE shall decode the received C&M link bit rates by looking at both Z.66.0 and Z.194.0. When the RE receives a valid or an updated bit rate in either Z.66.0 or Z.194.0 from the REC,

- If at least one of the currently received bit rates is equal to the corresponding bit rate sent by REC, the C&M plane setup is achieved
- If both currently received bit rates differ from the current bit rates sent by the RE the RE shall reselect the C&M bit rates for each C&M link, i.e. on both Z.66.0 and Z.194.0. The new proposed C&M bit rates shall be selected according to the rule:

New RE bit rate = highest available bit rate which is less or equal to received REC bit rate (received in Z.66.0 or Z.194.0)

Error case: The resulting bit rate according to the rule is “no link”, i.e. 0 bit rate:

New RE bit rate = lowest available bit rate

Note that the reselection may choose the already transmitted C&M bit rates. The new selected bit rates shall be stated in Z.66.0 and Z.194.0. If at least one of the currently received bit rates is equal to the corresponding new bit rate sent by RE, the C&M plane setup is achieved.

The RE shall check that Z.2.0 is equal in uplink and downlink. If it is not equal it shall enter state C.

Comments:

If the REC does not receive a new C&M bit rate proposal before the layer 1 start-up timer expires, it can assume that there are no common C&M bit rates on this line bit rate. Such a detection can be made faster but then the application must take into account the case where the RE enters the state after the REC. The negotiation results in a common C&M bit rate on at least one of the available C&M links. While in this state, L1 inband protocol is interpreted which may lead to state G being entered.

#### 4.5.3.5. State E – Interface and Vendor specific Negotiation

Prerequisites:

One C&M link speed is agreed on.

Description:

During this state, application in REC and RE negotiate the CPRI usage.

Interpreted control words:

All

REC actions:

If a common bit rate for the Ethernet link was agreed on in state D, it shall be used. Otherwise the HDLC link shall be used. The connection establishment and higher layer negotiation is outside the scope of the specification. When the connection is established the “layer 1 start-up timer” shall be cleared.

The REC shall check that Z.2.0 is equal in uplink and downlink. If it is not equal it shall enter state C. The REC shall check that at least one of the values Z.66.0 or Z.194.0 is equal in uplink and downlink. If both differ, it shall enter state D.

RE actions:

If a common bit rate for the Ethernet link was agreed on in state D, it shall be used. Otherwise the HDLC link shall be used. The connection establishment and higher layer negotiation is outside the scope of the specification. When the connection is established the “layer 1 start-up timer” shall be cleared.

The RE shall check that Z.2.0 is equal in uplink and downlink. If it is not equal it shall enter state C. The RE shall check that at least one of the values Z.66.0 or Z.194.0 is equal in uplink and downlink. If both differ, it shall enter state D.

Comments:

The REC and RE exchange information about capabilities and capability limitations resulting in a preferred configuration of the CPRI, including also the vendor specific parts. The negotiation and the corresponding C&M messages are not within the scope of the CPRI specification. The result of the negotiations may require

a reconfiguration of the RE or REC circuitry. Depending on the degree of change, the start up procedure may have to restart at state B, C or D, with a new set of characteristics (line bit rate, protocol, C&M speed).

#### 4.5.3.6. State F – Operation

Prerequisites:

The optimum supported C&M link is established. The use of the vendor specific area is agreed upon.

Description:

Normal operation.

Interpreted control words:

All

REC actions:

The REC shall check that Z.2.0 is equal in uplink and downlink. If it is not equal it shall enter state C. The REC shall check that at least one of the values Z.66.0 or Z.194.0 is equal in uplink and downlink. If both differ, it shall enter state D.

RE actions:

The RE shall check that Z.2.0 is equal in uplink and downlink. If it is not equal it shall enter state C. The RE shall check that at least one of the values Z.66.0 or Z.194.0 is equal in uplink and downlink. If both differ, it shall enter state D.

Comments:

In normal operation, the C&M plane has been established and all further setup of HW, functionality, user plane links, IQ format, etc is conducted using procedures outside the scope of the CPRI specification. If the CPRI is subject to a failure state, B is entered. If a reconfiguration is required state D may be entered.

#### 4.5.3.7. State G – Passive Link

Prerequisites:

Layer 1 is synchronized and the protocol is agreed on. REC does not propose any C&M interface.

Description:

The interface is not carrying the C&M plane

Interpreted control words:

All

REC actions:

While in this state, the REC shall set the C&M bit rates in Z.66.0 and Z.194.0 to 0. The REC shall check that Z.2.0 is equal in uplink and downlink. If not equal it shall enter state C.

RE actions:

While in this state, the RE shall set the C&M bit rates in Z.66.0 and Z.194.0 to the highest available bit rate. The RE shall check Z.2.0 is equal in uplink and downlink. If it is not equal it shall enter state C. The RE shall detect any change in the downlink value Z.66.0 or Z.194.0. If at least one value changes it shall enter state D.

Comments:

This state may be entered due to any of the following reasons:

The interface is used for redundancy and does not carry any information at the moment. Further setup is done on the active link.

The interface is used to expand the user plane capacity and its I&Q streams are part of the user plane. Further setup is done on the active link.

As a fallback, the REC may enable the C&M link by proposing a C&M link bit rate and the startup then enters state D. It is therefore important that the RE transmits a proper C&M bit rate.

## 4.5.4. Transition Description

### 4.5.4.1. Transition 1

Trigger:

The trigger is out of the scope of the CPRI specification. But it is required for the CPRI circuit initiation to be completed. A set of available line bit rates, protocol versions and C&M link bit rates shall be available. This may be the equipment full capabilities or a subset determined by the equipment configuration (manual) or knowledge from previous successful configurations. Such a subset will shorten the time in state B, C and D. Time and frequency references shall be predictive for the REC.

Actions:

None

### 4.5.4.2. Transition 2

Trigger:

First time the synchronization state HFNSYNC is entered. Received CPRI line bit rate is equal to transmitted CPRI line bit rate.

Actions:

The "layer 1 start-up timer" is set.

### 4.5.4.3. Transition 3

Trigger:

Protocol is agreed on. First time transmitted Z.2.0 is equal to received Z.2.0.

Actions:

None

### 4.5.4.4. Transition 4

Trigger:

The C&M link bit rate is agreed on. First time at least one of the two conditions below is fulfilled:

- Received Z.66.0 is equal to transmitted Z.66.0, and received Z.66.0 indicates a valid bit rate.
- Received Z.194.0 is equal to transmitted Z.194.0, and received Z.194.0 indicates a valid bit rate.

### 4.5.4.5. Transition 5

Trigger:

Out of the scope of the CPRI specification. Application has selected a new C&M link bit rate set and the C&M link bit rate is re-setup.

Actions:

The "layer 1 start-up timer" is set.

### 4.5.4.6. Transition 6

Trigger:

Out of the scope of the CPRI specification. The capability negotiation is accepted by both REC and RE applications and the present CPRI configuration is considered to be the best available choice.

Actions:

The "layer 1 start-up timer" is cleared.

### 4.5.4.7. Transition 7

Trigger:

Out of the scope of the CPRI specification. A capability update requiring CPRI capability renegotiation is performed by the applications.

Actions:

None

## 4.5.4.8. Transition 8

Trigger:

Out of the scope of the CPRI specification. The C&M plane connection is detected lost by the application due to fault or reconfiguration.

Actions:

The "layer 1 start-up timer" is set.

## 4.5.4.9. Transition 9

Trigger:

Out of the scope of the CPRI specification. The capability negotiation by the application proposes a new CPRI protocol or line bit rate.

Actions:

The transition carries information about the agreed available set of line bit rates, protocol versions and C&M bit rates. The "layer 1 start-up timer" is cleared.

## 4.5.4.10. Transition 10

Trigger:

First time LOS or LOF has been found faulty as defined in 4.2.10.

Actions:

The "layer 1 start-up timer" is cleared.

## 4.5.4.11. Transition 11

Trigger:

The RE or REC is powered on or reset. The reset of an RE may be controlled by C&M message or control bit in Z.130.0.

Actions:

The "layer 1 start-up timer" is cleared.

## 4.5.4.12. Transition 12

Trigger:

First time any of the received C&M bit rates in Z.66.0 or Z.194.0 is changed while in state E or F.

Actions:

The "layer 1 start-up timer" is set.

## 4.5.4.13. Transition 13

Trigger:

First time the received protocol version in Z.2.0 is changed while in stated D, E, F or G.

Actions:

The "layer 1 start-up timer" is set.

## 4.5.4.14. Transition 14

Trigger:

First time the REC has set the Z.66.0 and Z.194.0 to indicate that no C&M link is desired on the interface.

Actions:

The "layer 1 start-up timer" is cleared.



#### 4.5.4.15. Transition 15

Trigger:

First time the REC proposes C&M bit rates in at least one of Z.66.0 or Z.194.0.

Actions:

The “layer 1 start-up timer” is set.

#### 4.5.4.16. Transition 16

Trigger:

When “layer 1 start-up timer” expires.

Actions:

None

---

## 5. Interoperability

### 5.1. Forward and Backward Compatibility

#### 5.1.1. Fixing Minimum Control Information Position in CPRI Frame Structure

For forward and backward compatibility, the minimum control information position shall be fixed in the CPRI frame in order to find CPRI protocol version correctly. In later versions the position within CPRI hyperframe of the below listed bits shall not be changed:

- Sync and timing (control word: Z.0.0)
- Protocol version (control word: Z.2.0)
- HFN (control word: Z.64.0)

#### 5.1.2. Reserved Bandwidth within CPRI

Within the CPRI structure some data parts are reserved for future use. These parts may be used in future releases of the CPRI specification to enhance the capabilities or to allow the introduction of new features in a backward compatible way.

Two types of reserved blocks need to be distinguished:

##### Reserved Bits:

Reserved bits are marked with “r”. This means that a transmitter shall send 0’s for bits marked with “r”, and the receiver shall not interpret bits marked with “r” (transmit: r = 0, receiver: r = don’t care).

##### Reserved Control Words:

In the current version of the specification 52 control words (sub channels 3 to 15) of one hyperframe are reserved for future interface protocol extensions. Reserved words are completely filled with reserved bits (reserved bits are marked with “r”).

CPRI reserved data parts shall be used only for protocol enhancements/modifications by the CPRI specification group.

#### 5.1.3. Version Number

The CPRI specification version is indicated by two digits (version A.B). The following text defines the digits’:

- The first digit A is incremented to reflect significant changes (modification of the scope, new section...)
- The second digit B is incremented for all changes of substance, i.e. technical enhancements, corrections, updates, ...

#### 5.1.4. Specification Release Version mapping into CPRI Frame

The control word Z.2.0 indicates the protocol version number, which will be denoted by 1, 2, 3, ... The protocol version number will be incremented only when a new specification release version includes changes that lead to incompatibility with previous specification release versions. The simple sequence and the well-defined rule for non-compatibility between different specification release versions allow a simple, efficient and fast start-up procedure. The following table provides the initial mapping between specification release version and protocol version number.

Table 15: Specification release version and protocol version numbering

Specification release version	Compatible with the following previous specification release versions	Protocol version number (Z.2.0 control word)
1.0	-	1
1.1	1.0 *	1
1.2	1.0 *, 1.1	1
1.3	1.0 *, 1.1, 1.2	1
1.4	1.0 *, 1.1, 1.2, 1.3	1

\* The compatibility between V1.0 and the other specification release versions requires the V1.0 receiver to tolerate the /I1/ sequence as specified in section 4.2.7.5.

This table shall be updated when new specification release versions become available.

## 5.2. Compliance

A CPRI compliant interface application fulfils all following requirements:

- Establishes and maintains a connection between RE and REC by means of mandatory and optional parts of the CPRI specification.
- Establishes and maintains a connection between RE and REC by means of supporting all mandatory parts of CPRI specification.
- Establishes and maintains a connection between RE and REC by means of selecting at least one option out of every option list in the CPRI specification.
- Does not add any additional options in an option list.
- Does not add additional option lists.
- Does not produce errors when passing data between SAP's in RE and REC.

It is not required that all the CPRI compatible modules shall meet the full set of requirements defined in the section 3. The performances of the module can be restricted to a subset of the requirement when some application is not requiring the full performance of CPRI specification.

For each CPRI compatible module, the vendor shall explicitly give the compliance list for each item of the section 3 that are impacted by the module design even if the full specification requirement is not met.

## 6. Annex

### 6.1. Delay Calibration Example (Informative)

This section provides an example for the delay calibration procedure that has been described in Section 4.2.9.

The delay between REC and RE (**T12** and **T34**) can be estimated as follows.

Step 1) Measure **T14**, the frame timing difference between the output signal at **R1** and the input signal at **R4**. Assume  $\langle T14 \rangle$  is the measured value of **T14**.

Step 2) Estimate the round trip delay between REC and RE  $\langle T12+T34 \rangle$  by subtracting the known value **Toffset** from  $\langle T14 \rangle$ .  $\langle T12+T34 \rangle = \langle T14 \rangle - \text{Toffset}$

Step 3) If we can assume the downlink delay (**T12**) and the uplink delay (**T34**) is the same, then we can estimate the one way delay from the round-trip delay by halving it.

$$\langle T12 \rangle = \langle T34 \rangle = \langle T12+T34 \rangle / 2 = (\langle T14 \rangle - \text{Toffset}) / 2$$

As these two reference points **R1** and **R4** are in the same equipment, REC, it is feasible to measure the **T14** accurate enough to fulfil the requirement (R-21) in Section 3.6.

Of course it may be difficult to measure the timing at **R1** and **R4** directly because the signals at these points are optical or electrical high speed signals, but it is feasible to measure the timing difference somewhere in REC (e.g. before and after the SerDes) and to compensate the internal timing difference between measurement points and **R1/R4**.

As it is feasible enough to assume that REC knows the overall down link delay (**T2a**) and uplink delay (**Ta3**) in RE, REC can easily estimate the overall delay including the delay between REC and RE by adding  $\langle T12 \rangle$  and  $\langle T34 \rangle$ .

Where,

- **T2a** is the delay from the basic frame boundary of downlink signal at **R2** to the transmit timing at RE antenna (Ra) of the chip carried in the corresponding basic frame.
- **Ta3** is the delay from the received signal at RE antenna (Ra) to the frame boundary at **R3** in which basic frame the I/Q sample of the corresponding received signal is carried as the first I/Q sample.

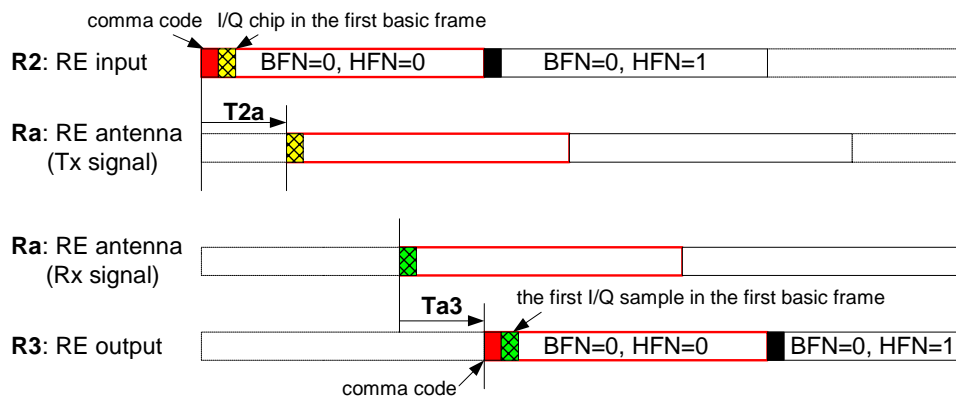


Figure 31: Definition of RE internal delay

## 6.2. Electrical Physical Layer Specification (Informative)

This section and all the following subsections are informative only.

Two electrical variants are recommended for CPRI usage denoted HV (high voltage) and LV (low voltage) in Figure 32. The HV variant is guided by 1000Base-CX electrical interface specified in Clause 39 of IEEE 802.3-2002 [ 1 ], but with 100Ω impedance and adapted to CPRI line bit rates. The LV variant is guided by the XAUI electrical interface specified in Clause 47 of IEEE 802.3ae-2002 [ 2 ], but adapted to CPRI line bit rates.

The intention is to be able to reuse electrical designs from XAUI or 1000BASE-CX, respectively.

All unit intervals are specified with a tolerance of +/- 100 ppm. The worst-case frequency difference between any transmit and receive clock will be 200 ppm. Note that this requirement is only aiming at achieving a data BER of  $10^{-12}$  through the CPRI link. The CPRI clock tolerance is driven by 3GPP requirements (see 3GPP TS 25.104 [ 8 ]).

### 6.2.1. Overlapping Rate and Technologies

Two different technologies can be used for CPRI with an overlap with respect to CPRI line bit rate ranges.

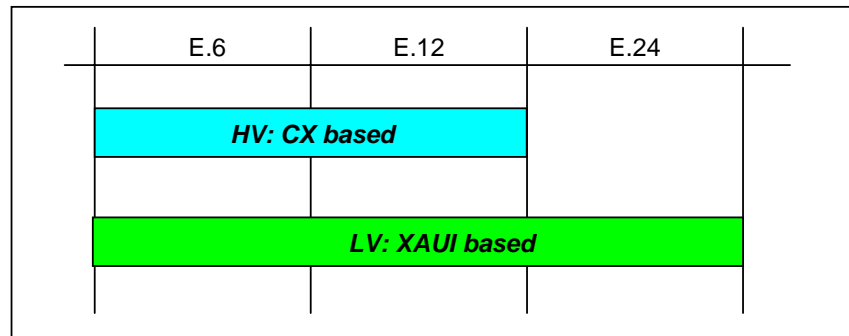


Figure 32: HV (high voltage) and LV (low voltage) electrical layer 1 usage

Nothing prevents from inter-operating the two electrical variants after “bi-lateral” tests. Neither does anything prevent from developing a circuit supporting both variants.

### 6.2.2. Signal Definition

The CPRI link uses differential signalling. Figure 33 defines terms used in the description and specification of the CPRI differential signal pair.

Caution shall be taken that some standards and IC data sheet define electrical characteristic with  $V_{diffpp}$  value, which is twice  $V_{diff}$ .

The single ended voltage swing is what is measured on one line of the paired differential signal.

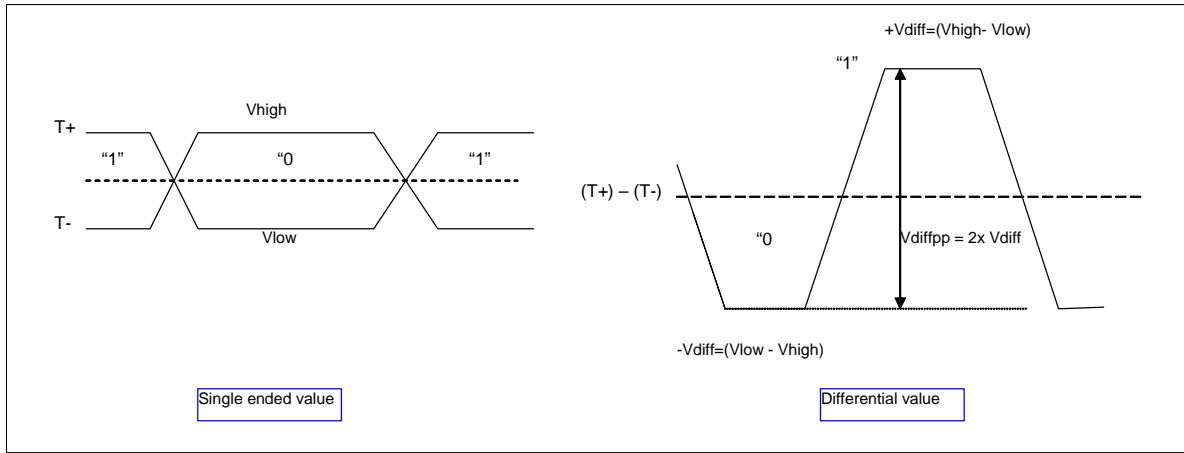


Figure 33: Definition of differential signals of a transmitter or receiver

### 6.2.3. Eye Diagram and Jitter

Jitter values and differential voltage levels at both Transmitter and Receiver are specified according to the reference eye diagram in Figure 34.

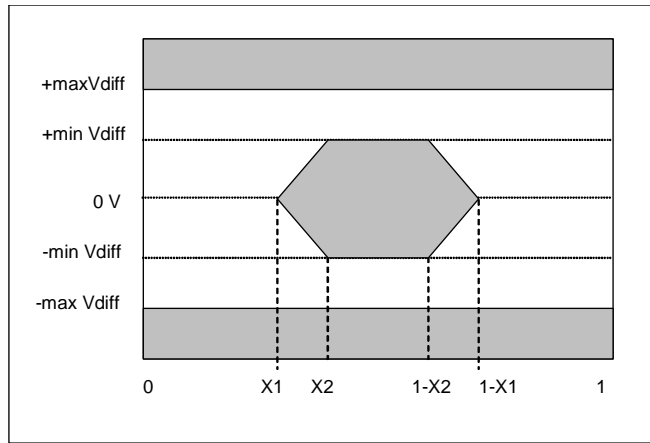


Figure 34: Definition of eye diagram mask

In addition, deterministic and total jitter budget values are specified.

### 6.2.4. Reference Test Points

Four reference test points are specified:

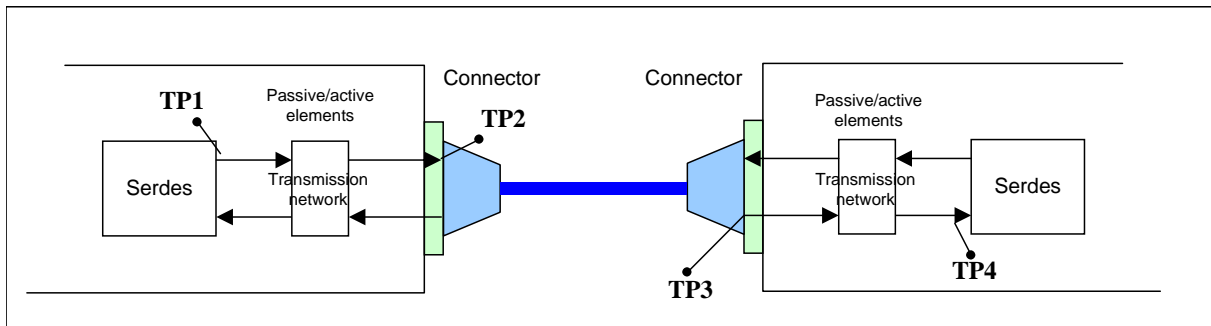


Figure 35: Reference test points

TX and RX requirements are specified at TP1 and TP4 respectively for the Low voltage electrical interface guided by XAUI. The characteristics of the channel between TP1 and TP4 are not included in the CPRI specification.

TX and RX requirement are specified at TP2 and TP3 respectively for the High voltage electrical interface guided by 1000Base-CX. The characteristics of the channel between TP2 and TP3 are not included in the CPRI specification.

### 6.2.5. Cable and Connector

Neither cable, nor PCB, nor connectors are specified for the CPRI.

### 6.2.6. Impedance

Two options are specified:

- Low Voltage variant: Guided by IEEE802.3ae [ 2 ], clause 47. The differential impedance of the channel is 100  $\Omega$ .
- High Voltage variant: Guided by IEEE 802.3 [ 1 ], clause 39, except that 150  $\Omega$  differential impedance is replaced by 100  $\Omega$ .

### 6.2.7. AC Coupling

Two options are specified:

- Low Voltage variant: Guided by IEEE802.3ae [ 2 ], clause 47. The link is AC coupled at the receiver side.
- High Voltage variant: Guided by IEEE 802.3 [ 1 ], clause 39. The link is AC coupled at the receiver side and optionally AC coupled at the transmitter side.

## 6.2.8. TX Performances

### 6.2.8.1. LV TX

The serial transmitter electrical and timing parameters for E.6.LV, E.12.LV and E.24.LV are stated in this section. All given TX parameters are referred to TP1. The TX parameters are guided by XAUI electrical interface (IEEE 802.3ae-2002 [ 2 ], clause 47).

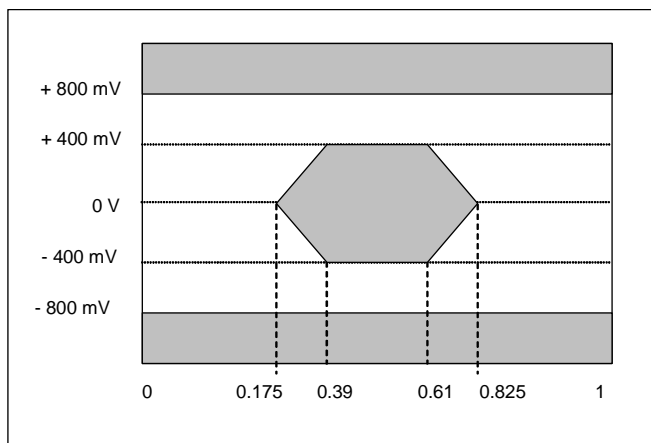


Figure 36: E.6.LV, E.12.LV, E.24.LV transmitter output mask

Table 16: E.6.LV, E.12.LV and E.24.LV transmitter AC timing specification

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Output Voltage	$V_o$	-0.40	2.30	Volts	Voltage relative to common of either signal comprising a differential pair
Differential Output Voltage	$V_{DIFFPP}$	800	1600	mV,p-p	
Deterministic Jitter	$J_D$		0.17	UI	
Total Jitter	$J_T$		0.35	UI	
Unit Interval E.6.LV	UI	1/614.4	1/614.4	$\mu$ s	+/- 100 ppm
Unit Interval E.12.LV	UI	1/1228.8	1/1228.8	$\mu$ s	+/- 100 ppm
Unit Interval E.24.LV	UI	1/2457.6	1/2457.6	$\mu$ s	+/- 100 ppm

The differential return loss,  $S_{11}$ , of the transmitter in each case shall be better than

-10 dB for  $[\text{CPRI line bit rate}/10] < f < 625 \text{ MHz}$ , and

-10 dB +  $10\log(f / (625 \text{ MHz})) \text{ dB}$  for  $625 \text{ MHz} \leq f \leq [\text{CPRI line bit rate}]$

The reference impedance for the differential return loss measurement is  $100 \Omega$  resistive. Differential return loss includes contribution from serdes on-chip circuitry, chip packaging and any off-chip components related to the driver. The output impedance requirement applies to all valid output levels.

It is recommended that the 20%-80% rise/fall time of the CPRI-LV Serial transmitter, as measured at the transmitter output, in each case have a minimum value of 60 ps.



It is recommended that the timing skew at the output of a CPRI-LV Serial transmitter between the two signals that comprise a differential pair does not exceed 15 ps.

### 6.2.8.2. HV TX

The TX electrical and timing parameters for E.6.HV and E.12.HV are stated in this section. All given TX parameters are referred to TP2. The TX parameters are guided by 1000Base-CX (IEEE 802.3-2002 [ 1 ], clause 39, PMD to PMI interface).

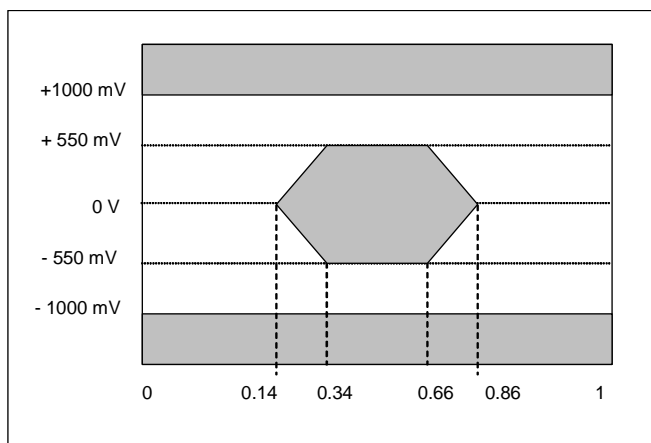


Figure 37: E.6.HV and E.12.HV transmitter mask

Table 17: E.6.HV and E.12.HV transmitter AC timing specification

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Differential Output Voltage	$V_{DIFFPP}$	1100	2000	mV,p-p	
Rise / Fall time (20% to 80 %)	$T_{RF}$	85	327	ps	
Deterministic Jitter	$J_D$		0.14	UI	
Total Jitter	$J_T$		0.279	UI	
Output skew	$S_O$		25	ps	
Unit Interval E.6.HV	UI	1/614.4	1/614.4	$\mu$ s	+/- 100 ppm
Unit Interval E.12.HV	UI	1/1228.8	1/1228.8	$\mu$ s	+/- 100 ppm

The differential return loss,  $S_{11}$ , of the transmitter in each case shall be better than

-15 dB for  $[CPRI \text{ line bit rate}/10] < f < 625 \text{ MHz}$ , and

-15 dB +  $10\log(f / (625 \text{ MHz}))$  dB for  $625 \text{ MHz} \leq f \leq [CPRI \text{ line bit rate}]$

The reference impedance for the differential return loss measurement is 100  $\Omega$  resistive. Differential return loss includes contribution from serdes on-chip circuitry, chip packaging and any off-chip components or transmission lines related to the driver transmission network. The output impedance requirement applies to all valid output levels.

### 6.2.8.3. Pre-emphasis and Equalization

Pre-emphasis is allowed by CPRI to overcome data dependent jitter issue. Neither specific pre-emphasis value nor other equalization technique is specified within CPRI.

The output eye pattern of a CPRI transmitter that implements pre-emphasis (to equalize the link and reduce inter-symbol interference) need only comply with the Transmitter Output Compliance Mask when pre-emphasis is disabled or minimized.

Pre-emphasis and Equalization techniques are to be tested on a bilateral end-to-end basis in between CPRI modules.

## 6.2.9. Receiver Performances

### 6.2.9.1. LV RX

The serial receiver electrical and timing parameters for E.6.LV, E.12.LV and E.24.LV are stated in this section. All given RX parameters are referred to TP4. The RX parameters are guided by XAUI (IEEE 802.3ae [ 2 ], section 47).

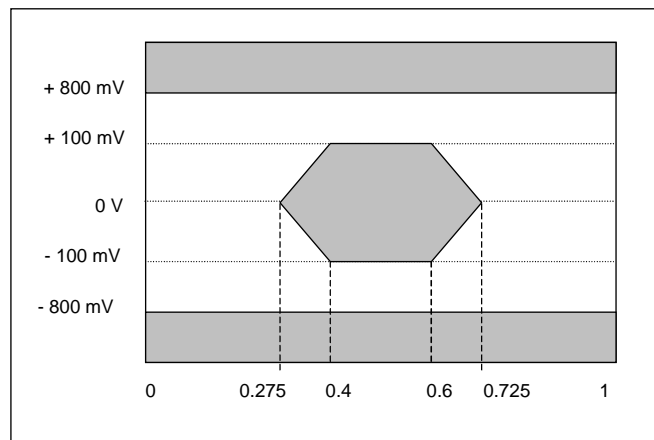


Figure 38: E.6.LV, E.12.LV and E.24.LV receiver mask

Table 18: E.6.LV, E.12.LV and E.24.LV receiver AC timing specification

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Differential Input Voltage	$V_{IN}$	200	1600	mV,p-p	Measured at receiver
Deterministic Jitter	$J_D$		0.37	UI	Measured at receiver
Combined Deterministic and Random Jitter	$J_{DR}$		0.55	UI	Measured at receiver
Total Jitter	$J_T$		0.65 <sup>1</sup>	UI	Measured at receiver
Bit Error Rate	BER		$10^{-12}$		
Unit Interval E.6.LV	UI	1/614.4	1/614.4	$\mu$ s	+/- 100 ppm
Unit Interval E.12.LV	UI	1/1228.8	1/1228.8	$\mu$ s	+/- 100 ppm
Unit Interval E.24.LV	UI	1/2457.6	1/2457.6	$\mu$ s	+/- 100 ppm

Note:

- Total random jitter is composed of deterministic jitter, random jitter and single frequency sinusoidal jitter. The sinusoidal jitter's amplitude and frequency is defined in agreement with XAUI specification IEEE 802.3ae-2002 [ 2 ], clause 47.

Input impedance is defined as 100 $\Omega$  and is tested by return loss measurement.

Receiver input impedance shall result in a differential return loss better than 10 dB and a common mode return loss better than 6 dB from [CPRI line bit rate/10] to [CPRI line bit rate] frequency. This includes contributions from on chip circuitry, the chip package and any off-chip components related to the receiver. AC coupling components are included in this requirement. The reference impedance for return loss measurements is 100 $\Omega$  resistive for differential return loss and 25  $\Omega$  resistive for common mode.

### 6.2.9.2. HV RX

The RX electrical and timing parameters for E.6.HV and E.12.HV are stated in this section. All given RX parameters are referred to TP3. The RX parameters are guided by 1000Base-CX (IEEE 802.3-2002 [ 1 ], clause 39, PMD to PMI interface).

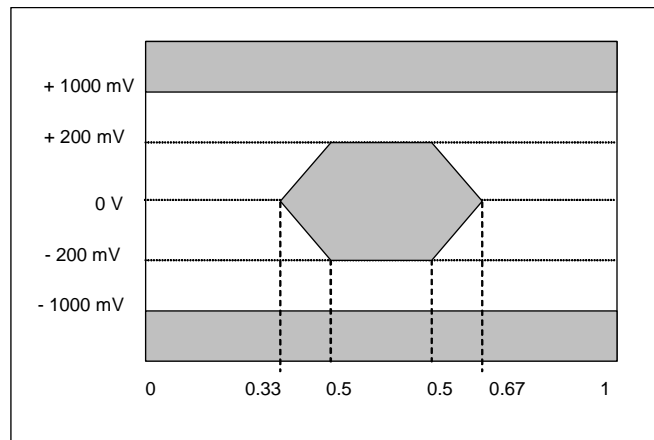


Figure 39: E.6.HV and E.12.HV receiver mask

Table 19: E.6.HV and E.12.HV receiver AC timing specification

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Differential Input Voltage	$V_{IN}$	400	2000	mV,p-p	
Deterministic Jitter	$J_D$		0.40	UI	
Total Jitter	$J_T$		0.66	UI	
Differential input skew	$S_I$		175	ps	
Bit Error Rate	BER		$10^{-12}$		
Unit Interval E.6.HV	UI	1/614.4	1/614.4	$\mu$ s	+/- 100 ppm
Unit Interval E.12.HV	UI	1/1228.8	1/1228.8	$\mu$ s	+/- 100 ppm

Input impedance is defined as  $100\Omega$  and is tested by return loss measurement.

Receiver input impedance shall result in a differential return loss better than 15 dB and a common mode return loss better than 6 dB from  $[CPRI \text{ line bit rate}/10]$  to  $[CPRI \text{ line bit rate}]$  frequency. This includes contributions from serdes on chip circuitry, the chip package and any off-chip components or transmission lines related to the receiver transmission network. AC coupling components are included in this requirement. The reference impedance for return loss measurements is  $100\Omega$  resistive for differential return loss and  $25\Omega$  resistive for common mode.

## 6.2.10. Measurement Procedure

CPRI does not provide means for physical layer conformance testing on chip level or CPRI module level. The measurement procedures shall be seen as recommendations for the chip manufacturers.

### 6.2.10.1. Low Voltage Option

Since the Low voltage electrical specification are guided by the XAUI electrical interface specified in Clause 47 of IEEE 802.3ae-2002 [ 2 ], the measurement and test procedures shall be similarly guided by Clause 47. In addition, the CJPAT test pattern defined in Annex 48A of IEEE802.3ae-2002 [ 2 ] restricted to lane 0 is specified as the test pattern for use in eye pattern and jitter measurements. Annex 48B of IEEE802.3ae-2002 [ 2 ] is recommended as a reference for additional information on jitter test methods.

### 6.2.10.2. High Voltage Option

Since the High voltage electrical specification are guided by the 1000Base-CX electrical interface specified in Clause 39 of IEEE 802.3-2002 [ 1 ], the measurement and test procedures shall be similarly guided by Clause 39, with the impedance value  $100\Omega$  instead of  $150\Omega$ . In addition, the CJPAT test pattern defined in Annex 48A of IEEE802.3ae-2002 [ 2 ] restricted to lane 0 is specified as the test pattern for use in eye pattern and jitter measurements. Annex 48B of IEEE802.3ae-2002 [ 2 ] is recommended as a reference for additional information on jitter test methods.

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## 7. List of Abbreviations

AC	Alternating Current
A/D	Analogue/Digital
ANSI	American National Standardization Institute
AxC	Antenna-carrier
BER	Bit Error Ratio
BFN	Node B Frame Number
C	Control
C&M	Control and Management
CPRI	Common Public Radio Interface
D/A	Digital/Analogue
DA	Destination Address
DL	Downlink
ESD	End-of-Stream-Delimiter
FCS	Frame Check Sequence
FDD	Frequency Division Duplex
GPS	Global Positioning System
HDLC	High-level Data Link Control
HFN	Hyper Frame Number
HV	High Voltage
I	In-Phase
IEC	International Electrotechnical Commission
IEEE	Institute of Electrical and Electronics Engineers
Iub	Interface between Radio Network Controller and UMTS radio base station (NodeB)
LLC	Logical Link Control
Ln	Length
LOF	Loss of Frame
LOS	Loss of Signal
LSB	Least Significant Bit
LV	Low Voltage
LVDS	Low Voltage Differential Signal
M	Management
MAC	Media Access Control
MSB	Most Significant Bit
PAD	Padding
PCS	Physical Coding Sublayer
PDU	Protocol Data Unit
PHY	Physical Layer
PMA	Physical Medium Attachment

Q	Quadrature
RAI	Remote Alarm Indication
RE	Radio Equipment
REC	Radio Equipment Control
RF	Radio Frequency
RRC	Root Raised Cosine
Rx	Receive
SA	Source Address
SAP	Service Access Point
SDI	SAP Defect Indication
SDU	Service Data Unit
SERDES	SerializerDeserialzer
SFD	Start-of-Frame Delimiter
SFP	Small Form-factor Pluggable
SSD	Start-of-Stream Delimiter
$T_c$	Chip rate = 1/3.84MHz
TP	Test Point
TS	Technical Specification
Tx	Transmit
UE	User Equipment
UL	Uplink
UTRA	Universal Terrestrial Radio Access (3GPP)
UTRAN	Universal Terrestrial Radio Access Network (3GPP)
UMTS	Universal Mobile Telecommunication System
Uu	UMTS air interface
XAUI	10 Gigabit Attachment Unit Interface
3GPP	3 <sup>rd</sup> Generation Partnership Project

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## 8. References

- [ 1 ] IEEE: Carrier sense multiple access with collision detection (CSMA/CD) access method and physical layer specifications. IEEE Std. 802.3-2002, March 2002.
- [ 2 ] IEEE Std 802.3ae-2002 "Part 3: Carrier sense multiple access with collision detection (CSMA/CD) access method and physical layer specifications Amendment: Media Access Control (MAC) Parameters, Physical Layers, and Management Parameters for 10 Gb/s Operation", March 2002.
- [ 3 ] INCITS 352 – Information Technology – Fibre Channel 1998 Physical Interface (FC-PI'98), 1998.
- [ 4 ] IEC 60793-2-10 (2002-3) Part 2-10: Product specifications Sectional specification for category A1 multimode fibres, March 2002.
- [ 5 ] IEC 60793-2-50 (2002-1) Part 2-50: Product specifications Sectional specification for class B single-mode fibres, January 2002.
- [ 6 ] Infiniband Trade Association: Infiniband Architecture, Rel. 1.1, Vol. 2, November 2002.
- [ 7 ] ANSI: ANSI-TIA-644, January 2001.
- [ 8 ] 3GPP TS 25.104: Base Station (BS) radio transmission and reception (FDD), Release 6, V 6.11.0, December 2005.
- [ 9 ] 3GPP TS 25.133: Requirements for support of radio resource management (FDD), Release 6, V 6.12.0, December 2005.
- [ 10 ] ISO/IEC: Information technology –Telecommunications and information exchange between systems – High-level data link control (HDLC) procedures. International Standard ISO/IEC 13239, 3<sup>rd</sup> edition, Reference number: ISO/IEC 13239:2002(E ), 2002-07-15.

## 9. History

Version	Date	Description
V 1.0	2003-09-30	First complete CPRI Specification
V 1.1	2004-05-10	<ul style="list-style-type: none"> <li>• Editorial corrections.</li> <li>• Section 3: Clarification of input requirements for CPRI.</li> <li>• Section 4.2.7.5: An additional sequence K28.5 + D5.6 (defined in the 8B/10B standard as /11/) is allowed for the use as control sync word to enable usage of existing SERDES devices.</li> <li>• Section 4.5.3.7: Editorial correction in subsection “RE actions” to align the text with Figure 30.</li> <li>• Section 5.1.4: Update of specification release version.</li> <li>• Section 5.2: Clarification of CPRI implementation compliancy.</li> </ul>
V 1.2	2004-07-15	<ul style="list-style-type: none"> <li>• Sections 4.2.2 to 4.2.4: Recommendation of a low voltage (CX based) and a high voltage (XAUI based) electrical interface</li> <li>• Addition of Section 6.2</li> <li>• Editorial changes and abbreviation addition</li> </ul>
V 1.3	2004-10-01	<p>Major editorial correction in Section 4.5.4.4 and Section 4.5.4.12:</p> <ul style="list-style-type: none"> <li>• Exchange of BYTE index Z.64.0 with Z.66.0</li> <li>• Exchange of BYTE index Z.192.0 with Z.194.0</li> </ul>
V 1.4	2006-03-31	<p>Chapters 1, 3, and 8:</p> <ul style="list-style-type: none"> <li>• Update of the scope and the requirement no. R-1 as well as of References [ 8 ] and [ 9 ] to 3GPP UTRA FDD, Release 6, December 2005</li> </ul> <p>Minor editorial correction in Section 4.2.7.5:</p> <ul style="list-style-type: none"> <li>• Table 9: Change X to 0    #Z.0.0 #Z.0.1 #Z.0.2 #Z.0.3</li> </ul>