CPRI Specification V6.1 (2014-07-01)

Interface Specification

Common Public Radio Interface (CPRI); Interface Specification

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1. Introduction

The Common Public Radio Interface (CPRI) is an industry cooperation aimed at defining a publicly available specification for the key internal interface of radio base stations between the Radio Equipment Control (REC) and the Radio Equipment (RE). The parties cooperating to define the specification are Ericsson AB, Huawei Technologies Co. Ltd, NEC Corporation, Alcatel Lucent and Nokia Networks.

Motivation for CPRI:

The CPRI specification enables flexible and efficient product differentiation for radio base stations and independent technology evolution for Radio Equipment (RE) and Radio Equipment Control (REC).

Scope of Specification:

The necessary items for transport, connectivity and control are included in the specification. This includes User Plane data, Control and Management Plane transport mechanisms, and means for synchronization.

A focus has been put on hardware dependent layers (layer 1 and layer 2). This ensures independent technology evolution (on both sides of the interface), with a limited need for hardware adaptation. In addition, product differentiation in terms of functionality, management, and characteristics is not limited.

With a clear focus on layer 1 and layer 2 the scope of the CPRI specification is restricted to the link interface only, which is basically a point to point interface. Such a link shall have all the features necessary to enable a simple and robust usage of any given REC/RE network topology, including a direct interconnection of multi-port REs.

Redundancy mechanisms are not described in the CPRI specification, however all the necessary features to support redundancy, especially in system architectures providing redundant physical interconnections (e.g. rings) are defined.

The specification has the following scope (with reference to Figure 1):

1. A digitized and serial internal radio base station interface that establishes a connection between 'Radio Equipment Control' (REC) and 'Radio Equipment' (RE) enabling single-hop and multi-hop topologies is specified.[1]
2. Three different information flows (User Plane data, Control and Management Plane data, and Synchronization Plane data) are multiplexed over the interface.
3. The specification covers layers 1 and 2.
   3a. The physical layer (layer 1) supports both an electrical interface (e.g., what is used in traditional radio base stations), and an optical interface (e.g. for radio base stations with remote radio equipment).
   3b. Layer 2 supports flexibility and scalability.

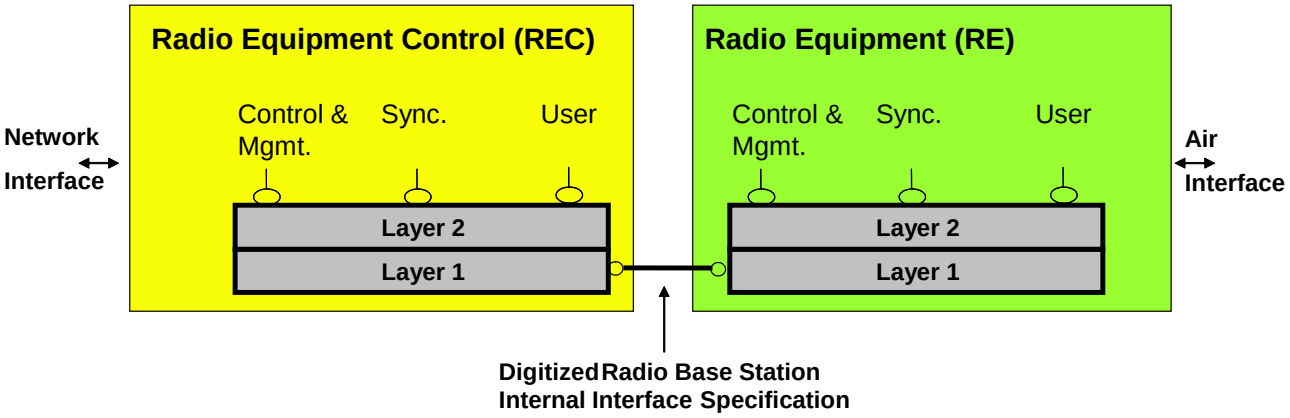


Figure 1: System and Interface Definition

[1] The CPRI specification may be used for any internal radio base station interface that carries the information flows mentioned in the scope of point 2.

2. System Description

This chapter describes the CPRI related parts of the basic radio base station system architecture and defines the mapping of the functions onto the different subsystems. Furthermore, the reference configurations and the basic nomenclature used in the following chapters are defined.

The following description is based on the UMTS (Universal Mobile Telecommunication System), WiMAX Forum Mobile System Profile [11] based on IEEE Std 802.16-2009 [13], Evolved UMTS Terrestrial Radio Access (E-UTRA), and GSM. However, the interface may also be used for other radio standards.

2.1. Definitions/Nomenclature

This section provides the basic nomenclature that is used in the following chapters.

Subsystems:

The radio base station system is composed of two basic subsystems, the radio equipment control and the radio equipment (see Figure 1). The radio equipment control and the radio equipment are described in the following chapter.

Node:

The subsystems REC and RE are also called nodes, when either an REC or an RE is meant. The Radio Base Station system shall contain at least two nodes, at least one of each type; REC and RE.

Protocol layers:

This specification defines the protocols for the physical layer (layer 1) and the data link layer (layer 2).

Layer 1 defines:

- Electrical characteristics
- Optical characteristics
- Time division multiplexing of the different data flows
- Low level signalling

Layer 2 defines:

- Media access control
- Flow control
- Data protection of the control and management information flow

Protocol data planes:

The following data flows are discerned:

Control Plane:	Control data flow used for call processing.
Management Plane:	This data is management information for the operation, administration and maintenance of the CPRI link and the nodes.
User Plane:	Data that has to be transferred from the radio base station to the mobile station and vice versa.
Synchronization:	Data flow which transfers synchronization and timing information between nodes.

The control plane and management plane are mapped to a Service Access Point SAP_{CM} as described below.

User plane data:

- For base stations with a functional decomposition according to section 2.4, the user plane data is transported in the form of IQ data. Several IQ data flows are sent via one physical CPRI link. Each IQ data flow reflects the data of one antenna for one carrier, the so-called antenna-carrier (AxC).
- For base stations with a functional decomposition different from section 2.4, the user plane data may not be IQ data.

Antenna-carrier (AxC):

One antenna-carrier is the amount of digital baseband (IQ) U-plane data necessary for either reception or transmission of only one carrier at one independent antenna element.

Control data stream for Antenna Carrier (Ctrl_AxC):

A Ctrl_AxC designates one AxC specific control data stream. Two bytes per hyperframe are reserved for each Ctrl_AxC as shown in section 4.2.7.10. For CPRI line bit rate option 1 (614.4 Mbps) in total eight Ctrl_AxCs are available while for higher line bit rates this number increases proportionally. The mapping of Ctrl_AxCs with number Ctrl_AxC# to AxCs as well as the actual content of the control data bytes are not defined in CPRI but are vendor specific.

Antenna-carrier (AxC) Group:

An **AxC Group** is an aggregation of N_A AxC with the same sample rate, the same sample width, the same destination SAP_{IQ}, and the same radio frame length. In case of N_A=1 an **AxC Group** is the same as an AxC.

AxC Container:

An **AxC Container** is a sub-part of the IQ data block of one basic frame. The size of an AxC Container is always an even number of bits. The mapping of AxC Containers into the basic frame is specified in section 4.2.7.2.3.

- For base stations with a functional decomposition according to section 2.4 the content of AxC Containers is defined below:
  - An AxC Container for UTRA-FDD contains the IQ samples of one AxC for the duration of one UMTS chip.
  - An AxC Container for WiMAX contains IQ sample bits of one AxC and sometimes also stuffing bits.
  - An AxC Container for E-UTRA contains one or more IQ samples for the duration of one UMTS chip or it contains IQ sample bits and sometimes also stuffing bits.
  - An AxC Container for GSM contains IQ sample bits of one AxC and sometimes also stuffing bits.
- For base stations with a functional decomposition different from section 2.4 an AxC Container contains user plane data that may not be IQ data. This means that the content, the format and the mapping of user plane data within the AxC Container are vendor specific and are not further specified within this specification. In this case an AxC Container does not necessarily relate to one AxC. The term “AxC Container” is used here for simplicity reasons, since the same rules for the size and the mapping into the basic frame apply.

AxC Container Group:

An **AxC Container Group** is an aggregation of N_C **AxC Containers** containing IQ samples for an **AxC Group** in one basic frame. N_C is defined in section 4.2.7.2.7.

AxC Symbol Block:

An **AxC Symbol Block** is an aggregation in time of N_{SAM} IQ samples for one WiMAX symbol plus N_{S_SYM} stuffing bits. N_{SAM} and N_{S_SYM} are defined in section 4.2.7.2.6.

AxC Container Block:

An **AxC Container Block** is an aggregation in time of *K* **AxC Container Groups** or an aggregation in time of N_{SYM} **AxC Symbol Blocks** plus N_{S_FRM} stuffing bits**.** It contains *S* IQ samples per AxC plus stuffing bits. *K* and *S* are defined in section 4.2.7.2. N_{SYM} and N_{S_FRM} are defined in section 4.2.7.2.6.

Service Access Points:

For all protocol data planes, layer 2 service access points are defined that are used as reference points for performance measurements. These service access points are denoted as SAP_{CM}, SAP_S and SAP_{IQ} as illustrated in Figure 2. A service access point is defined on a per link basis.

Stuffing bits:

Stuffing bits are used for alignment of WiMAX/E-UTRA/GSM sample frequencies to the basic frame frequency. Stuffing bits are also sent in TDD mode during time intervals when there is no IQ data to be sent over CPRI. The content of stuffing bits is vendor specific (“v”).

Stuffing samples:

If the total sampling rate per **AxC Group** is not the integer multiple of the CPRI basic frame rate (3.84MHz), then stuffing samples are added to make the total sampling rate the integer multiple of the CPRI basic frame rate. Stuffing samples are filled with vendor specific bits ("v").

Link:

The term "link" is used to indicate the bidirectional interface in between two directly connected ports, either between REC and RE, or between two nodes, using one transmission line per direction. A working link consists of a master port, a bidirectional cable, and a slave port.

Master/master and slave/slave links are not covered by this specification (for the definition of master and slave see below).

Passive Link:

A passive link does not support any C&M channel, i.e. it carries only IQ data and synchronization information. It may be used for capacity expansion or redundancy purposes, or for any other internal interfaces in a radio base station.

Hop:

A "hop" is the aggregation of all links directly connecting two nodes.

Multi-hop connection:

A "multi-hop connection" is composed of a set of continuously connected hops starting from the REC and ending at a particular RE including nodes in between.

Logical connection:

A "logical connection" defines the interconnection between a particular SAP (e.g., SAP_{CM}) belonging to a port of the REC and the corresponding peer SAP (e.g., SAP_{CM}) belonging to a port of one particular RE and builds upon a single hop, or a multi-hop connection, between the REC and that particular RE. Logical connections for C&M data, user plane data and synchronization can be distinguished.

Master port and slave port:

Each link connects two ports which have asymmetrical functions and roles: a master and a slave.

This is implicitly defined in CPRI release 1 with the master port in the REC and the slave port in the RE.

This master/slave role split is true for the following set of flows of the interface:

- Synchronization
- C&M channel negotiation during start-up sequence
- Reset indication
- Start-up sequence

Such a definition allows the reuse of the main characteristic of the CPRI release 1 specification, where each link is defined with one termination being the master port and the other termination being the slave port.

At least one REC in a radio base station shall have at least one master port and optionally have other ports that may be slave or master.

An RE shall have at least one slave port and optionally have other ports that may be slave or master.

Under normal conditions a link has always one master port and one slave port. Two master ports or two slave ports connected together is an abnormal situation and is therefore not covered by this specification.

Downlink:

Direction from REC to RE for a logical connection.

Uplink:

Direction from RE to REC for a logical connection.

Figure 1A and Figure 1B illustrate some of the definitions.

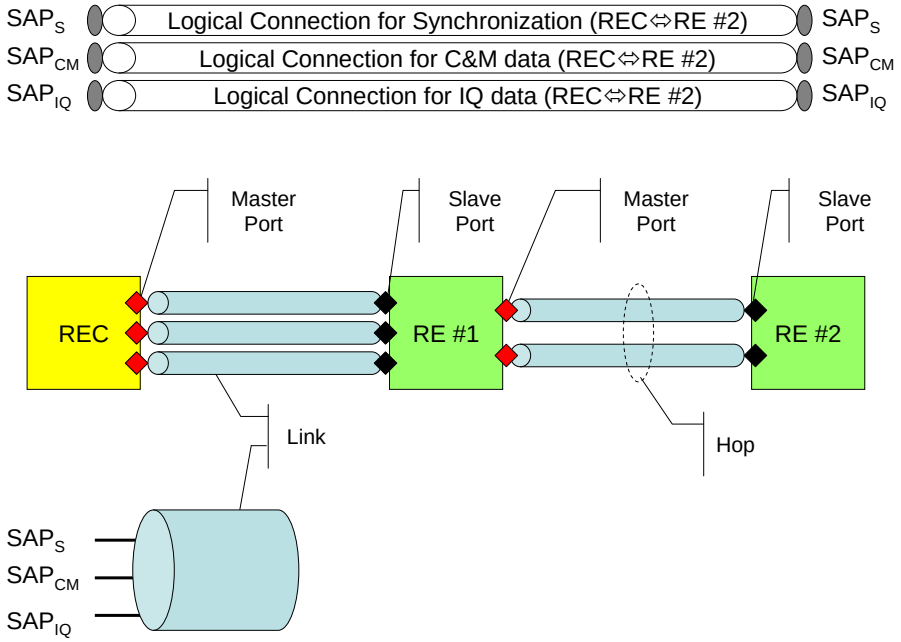


Figure 1A: Illustration of basic definitions

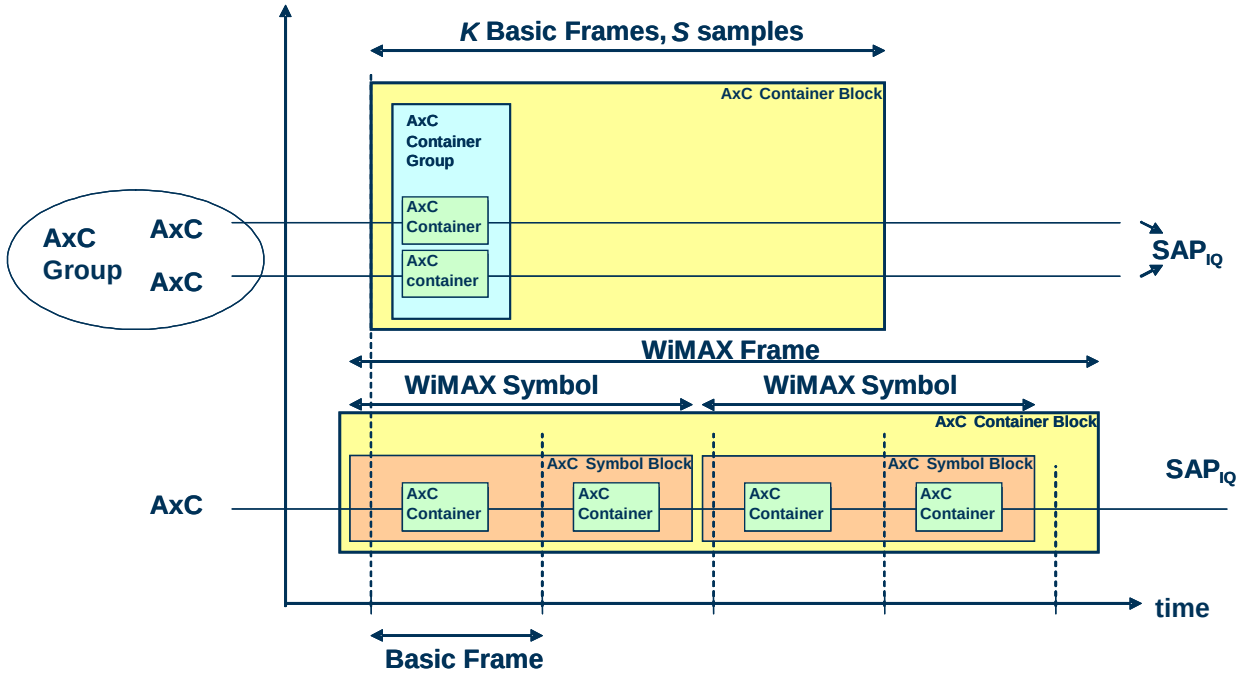


Figure 1B: Illustration of AxC related definitions

2.2. System Architecture

Radio base stations should provide deployment flexibility for the mobile network operators, i.e., in addition to a concentrated radio base station, more flexible radio base station system architectures involving remote radio equipment shall be supported. This may be achieved by a decomposition of the radio base station into two basic building blocks, the so-called radio equipment control (REC) and the radio equipment (RE) itself. Both parts may be physically separated (i.e., the RE may be close to the antenna, whereas the REC is located in a conveniently accessible site) or both may be co-located as in a conventional radio base station design.

The REC contains the radio functions of the digital baseband domain, whereas the RE contains the analogue radio frequency functions. The functional split between both parts is done in such a way that a generic interface based on In-Phase and Quadrature (IQ) data can be defined.

For the UMTS radio access network, the REC provides access to the Radio Network Controller via the Iub interface, whereas the RE serves as the air interface, called the Uu interface, to the user equipment.

For WiMAX, the REC provides access to network entities (e.g. other BS, ASN-GW), whereas the RE serves as the air interface to the subscriber station / mobile subscriber station (SS / MSS).

For E-UTRA, the REC provides access to the Evolved Packet Core for the transport of user plane and control plane traffic via S1 interface, whereas the RE serves as the air interface to the user equipment.

For GSM, the REC provides access to the Base Station Controller via the Abis interface, whereas the RE serves as the air interface, called the Um interface, to the mobile station.

A more detailed description of the functional split between both parts of a radio base station system is provided in Section 2.4.

In addition to the user plane data (IQ data), control and management as well as synchronization signals have to be exchanged between the REC and the RE. All information flows are multiplexed onto a digital serial communication line using appropriate layer 1 and layer 2 protocols. The different information flows have access to the layer 2 via appropriate service access points. This defines the common public radio interface illustrated in Figure 2. The common public radio interface may also be used as a link between two nodes in system architectures supporting networking. An example of a common public radio interface between two REs is illustrated in Figure 2A.

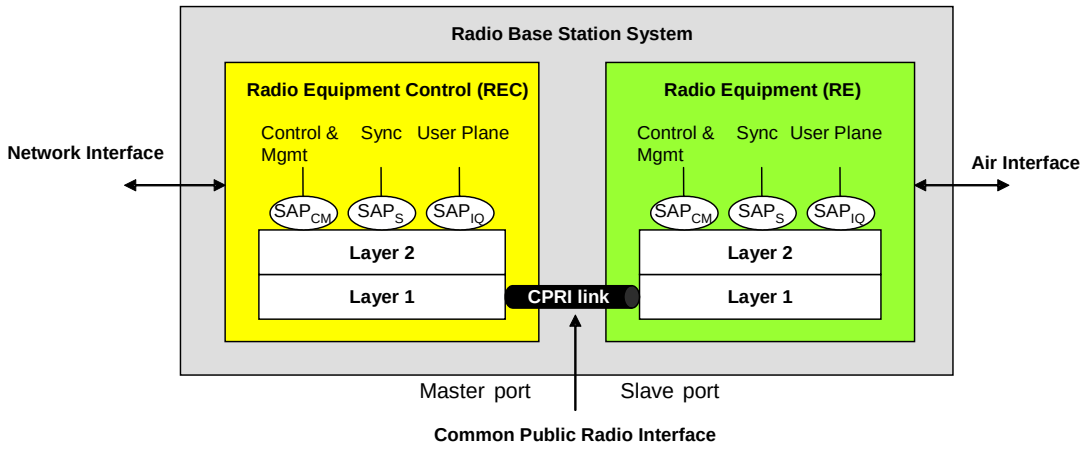


Figure 2: Basic System Architecture and Common Public Radio Interface Definition

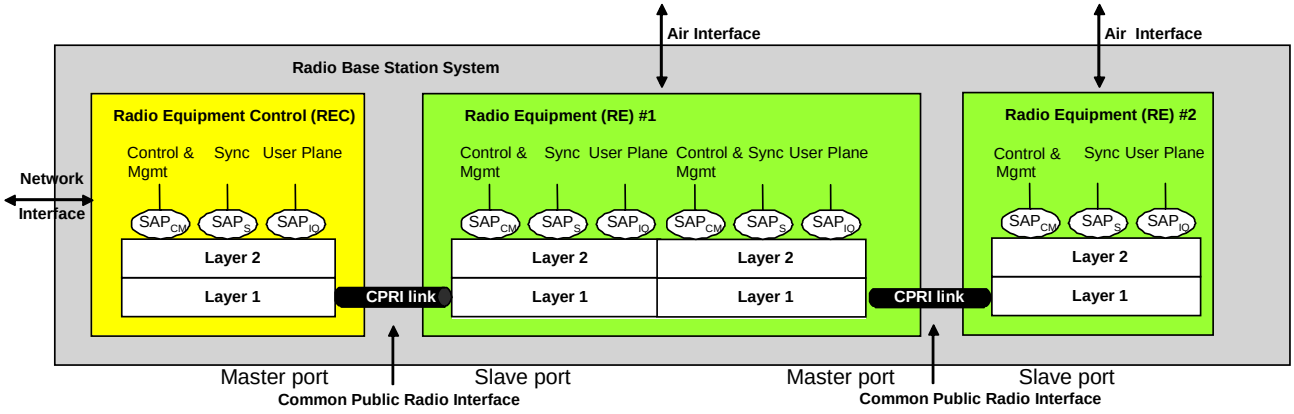


Figure 2A: System Architecture with a link between REs

2.3. Reference Configurations

This section provides the reference configurations that have to be supported by the CPRI specification. The basic configuration, shown in Figure 3, is composed of one REC and one RE connected by a single CPRI link. The basic configuration can be extended in several ways:

- First, several CPRI links may be used to enhance the system capacity as required for large system configurations involving many antennas and carriers (see Figure 4). It is required that an IQ data flow of a certain antenna and a certain antenna-carrier (see Section 2.1) is carried completely by one CPRI link (however, it is allowed that the same antenna-carrier may be transmitted simultaneously over several links). Therefore, the number of physical links is not restricted by this specification.
- Second, several REs may be served by one REC as illustrated in Figure 5 for the so-called star topology.
- Third, one RE may be served by multiple RECs as illustrated in Figure 5D. The requirements for this configuration are not fully covered in the CPRI specification; refer to section 6.3.7 for further explanation.
- Furthermore, three basic networking topologies may be used for the interconnection of REs:
    - Chain topology, an example is shown in Figure 5A
    - Tree topology, an example is shown in Figure 5B
    - Ring topology, an example is shown in Figure 5C
- Any other topology (e.g. combination of RECs and REs in a chain and tree) is not precluded. An example of reusing the CPRI interface for other internal interfaces in a radio base station is depicted in Figure 5E.
    - If a radio base station has multiple RECs, e.g. of different radio access technologies, the CPRI interface may be used for the interface between two RECs.
    - The requirements for this configuration are not fully covered in the CPRI specification; refer to sections 6.3.7 and 6.3.8 for further explanation.

Figure 3: Single point-to-point link between one REC and one RE

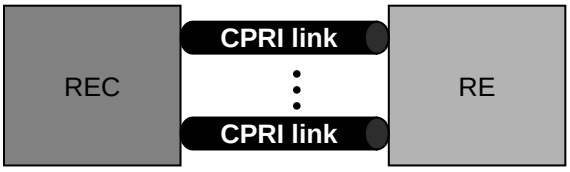


Figure 4: Multiple point-to-point links between one REC and one RE

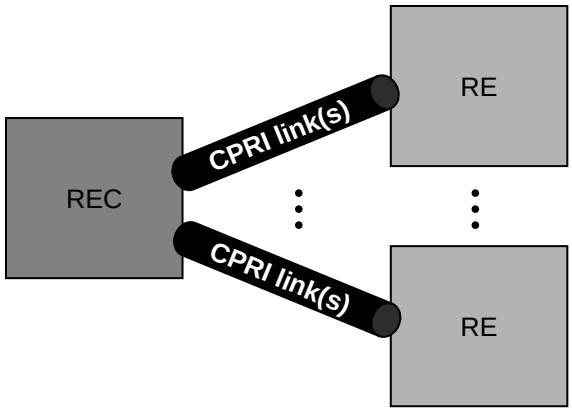


Figure 5: Multiple point-to-point links between one REC and several REs (star topology)

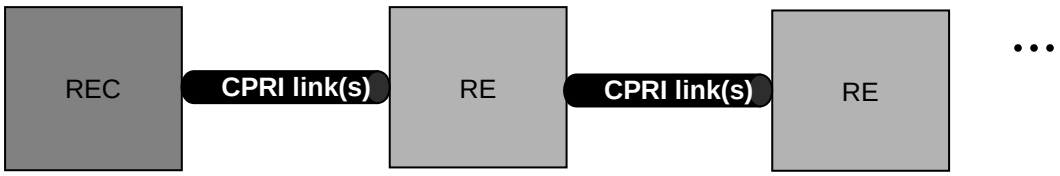


Figure 5A: Chain topology

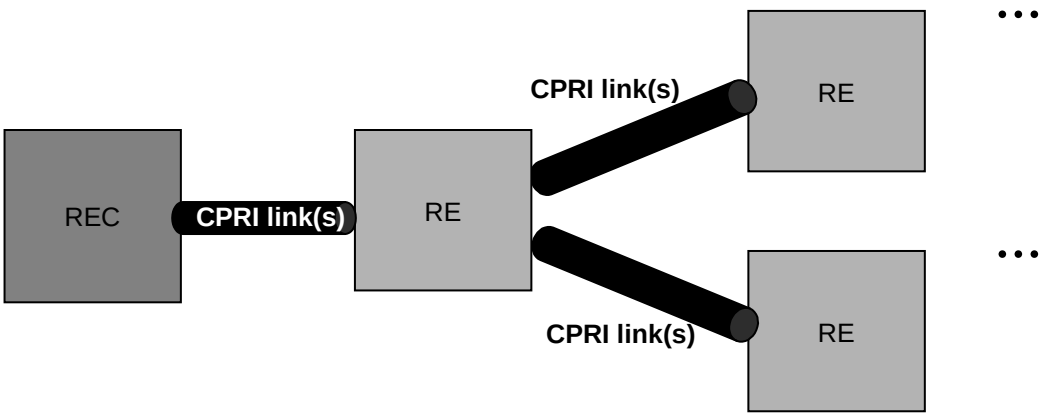


Figure 5B: Tree topology

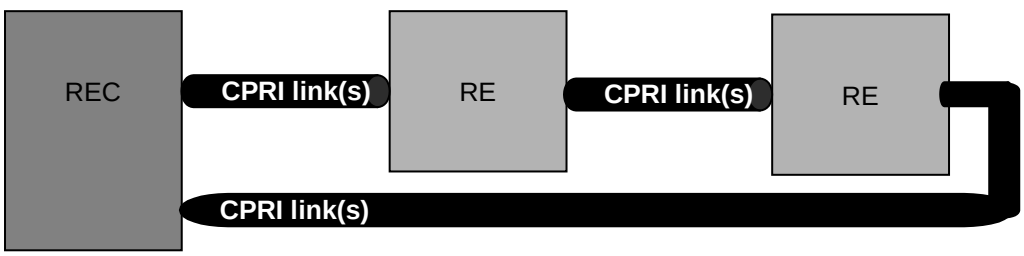


Figure 5C: Ring topology

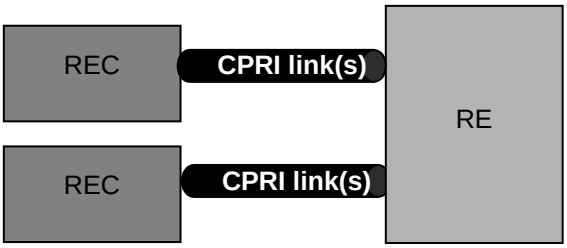


Figure 5D: Multiple point-to-point links between several RECs and one RE

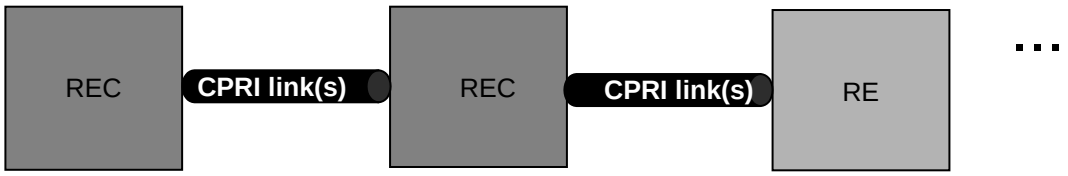


Figure 5E: Chain topology of multiple RECs

2.4. Functional Description

2.4.1. Radio Functionality

This section provides a more detailed view on the functional split between REC and RE, which provides the basis for the requirement definition in the next chapter.

The REC is concerned with the Network Interface transport, the radio base station control and management as well as the digital baseband processing. The RE provides the analogue and radio frequency functions such as filtering, modulation, frequency conversion and amplification. An overview on the functional separation between REC and RE is given in Table 1 for UTRA FDD, in Table 1A for WiMAX and E-UTRA and in Table 1AA for GSM. A functional split of base stations that is different from this section is not precluded by the CPRI specification.

Table 1: Functional decomposition between REC and RE (valid for the UTRA FDD standard)

Functions of REC		Functions of RE	
Downlink	Uplink	Downlink	Uplink
Radio base station control & management			
Iub transport		RRC Channel Filtering	
Iub Frame protocols		D/A conversion	A/D conversion
Channel Coding	Channel De-coding	Up Conversion	Down Conversion
Interleaving	De-Interleaving	ON/OFF control of each carrier	Automatic Gain Control
Spreading	De-spreading	Carrier Multiplexing	Carrier De-multiplexing
Scrambling	De-scrambling	Power amplification and limiting	Low Noise Amplification
MIMO processing			
Adding of physical channels	Signal distribution to signal processing units	Antenna supervision	
Transmit Power Control of each physical channel	Transmit Power Control & Feedback Information detection	RF filtering	RF filtering
Frame and slot signal generation (including clock stabilization)			
Measurements		Measurements	

Table 1A: Functional decomposition between REC and RE (valid for WiMAX & E-UTRA)

Functions of REC		Functions of RE	
Downlink	Uplink	Downlink	Uplink
Radio base station control & management		Add CP (optional)	
Backhaul transport		Channel Filtering	
MAC layer		D/A conversion	A/D conversion
Channel Coding, Interleaving, Modulation	Channel De-coding, De-Interleaving, Demodulation	Up Conversion	Down Conversion
iFFT	FFT	ON/OFF control of each carrier	Automatic Gain Control
Add CP (optional)	Remove CP	Carrier Multiplexing	Carrier De-multiplexing
MIMO processing		Power amplification and limiting	Low Noise Amplification
Signal aggregation from signal processing units	Signal distribution to signal processing units	Antenna supervision	
Transmit Power Control of each physical channel	Transmit Power Control & Feedback Information detection	RF filtering	RF filtering
Frame and slot signal generation (including clock stabilization)		TDD switching in case of TDD mode	
Measurements		Measurements	

Table 1AA: Functional decomposition between REC and RE (valid for the GSM standard)

Functions of REC		Functions of RE	
Downlink	Uplink	Downlink	Uplink
Radio base station control & management			
Channel Filtering		Channel Filtering	
Abis transport		D/A conversion	A/D conversion
Abis Frame protocols		Up Conversion	Down Conversion
Channel Coding	Channel De-Coding	ON/OFF control for each carrier	Automatic Gain Control
Interleaving	De-Interleaving	Carrier Multiplexing	Carrier De-multiplexing
Modulation	De-Modulation	Power amplification	Low Noise Amplification
Frequency hopping control		Frequency hopping	
Signal aggregation from signal processing units	Signal distribution to signal processing units	Antenna supervision	
Transmit Power Control of each physical channel	Transmit Power Control & Feedback Information detection	RF filtering	RF filtering
Frame and slot signal generation (including clock stabilization)			
Measurements		Measurements	

2.4.2. CPRI Control Functionality

This section provides a more detailed view on the functional split between REC and RE for CPRI functionality beyond the specification itself.

Basically, the REC is concerned with the management of the CPRI and the CPRI topology. The RE may optionally provide interconnection functionality between REs. An overview of the functional separation between REC and RE is given in Table 1B.

Table 1B: Functional decomposition between REC and RE (valid for CPRI control functionality)

Functions of REC		Functions of RE	
Downlink	Uplink	Downlink	Uplink
CPRI control management			
CPRI topology management		CPRI interconnection between REs (forwarding/switching/cross-connecting of CPRI SAP data between REs)	

3. Interface Baseline

The input requirements for the development of the CPRI specification are noted in Informative Annex B.

4. Interface Specification

4.1. Protocol Overview

CPRI defines the layer 1 and layer 2 protocols for the transfer of user plane, C&M as well as synchronization information between REC and RE as well as between two REs[2]. The interface supports the following types of information flows:

- IQ Data: User plane information in the form of in-phase and quadrature modulation data (digital baseband signals).
- Synchronization: Synchronization data used for frame and time alignment.
- L1 Inband Protocol: Signalling information that is related to the link and is directly transported by the physical layer. This information is required, e.g. for system start-up, layer 1 link maintenance and the transfer of time critical information that has a direct time relationship to layer 1 user data.
- C&M data: Control and management information exchanged between the control and management entities within the REC and the RE. This information flow is given to the higher protocol layers.
- Protocol Extensions: This information flow is reserved for future protocol extensions. It may be used to support, e.g., more complex interconnection topologies or other radio standards.
- Vendor Specific Information: This information flow is reserved for vendor specific information.

The user plane information is sent in the form of IQ data. The IQ data of different antenna carriers are multiplexed by a time division multiplexing scheme onto an electrical or optical transmission line. The control and management data are either sent as inband protocol (for time critical signalling data) or by layer 3 protocols (not defined by CPRI) that reside on top of appropriate layer 2 protocols. Two different layer 2 protocols for C&M data – subset of High level Data Link Control (HDLC) and Ethernet – are supported by CPRI. These additional control and management data are time multiplexed with the IQ data. Finally, additional time slots are available for the transfer of any type of vendor specific information. Figure 6 provides an overview on the basic protocol hierarchy.

[2] The CPRI protocol may be reused for any internal radio base station interfaces.

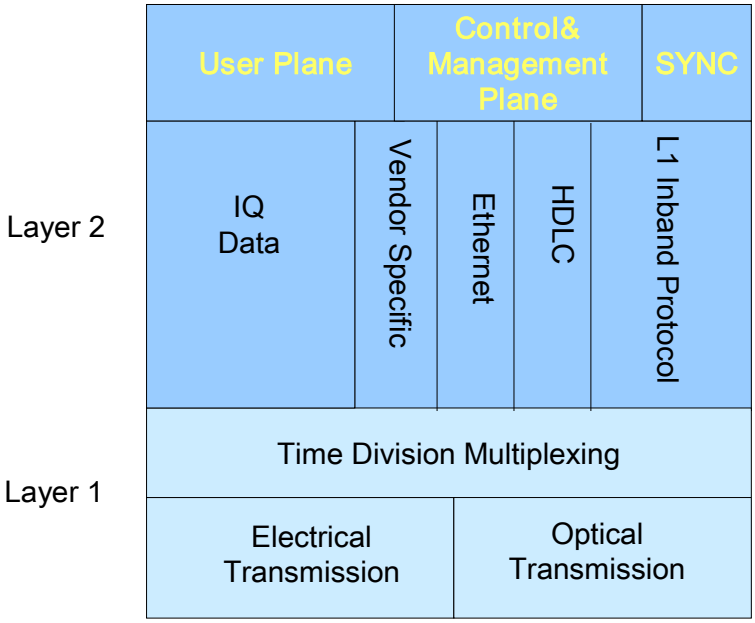


Figure 6: CPRI protocol overview

4.2. Physical Layer (Layer 1) Specification

4.2.1. Line Bit Rate

In order to achieve the required flexibility and cost efficiency, several different line bit rates are defined. Therefore, the CPRI line bit rate may be selected from the following option list:

- CPRI line bit rate option 1: 614.4 Mbit/s, 8B/10B line coding (1 x 491.52 x 10/8 Mbit/s)
- CPRI line bit rate option 2: 1228.8 Mbit/s, 8B/10B line coding (2 x 491.52 x 10/8 Mbit/s)
- CPRI line bit rate option 3: 2457.6 Mbit/s, 8B/10B line coding (4 x 491.52 x 10/8 Mbit/s)
- CPRI line bit rate option 4: 3072.0 Mbit/s, 8B/10B line coding (5 x 491.52 x 10/8 Mbit/s)
- CPRI line bit rate option 5: 4915.2 Mbit/s, 8B/10B line coding (8 x 491.52 x 10/8 Mbit/s)
- CPRI line bit rate option 6: 6144.0 Mbit/s, 8B/10B line coding (10 x 491.52 x 10/8 Mbit/s)
- CPRI line bit rate option 7: 9830.4 Mbit/s, 8B/10B line coding (16 x 491.52 x 10/8 Mbit/s)
- CPRI line bit rate option 7A: 8110.08 Mbit/s, 64B/66B line coding (16 x 491.52 x 66/64 Mbit/s)
- CPRI line bit rate option 8: 10137.6 Mbit/s, 64B/66B line coding (20 x 491.52 x 66/64 Mbit/s)
- CPRI line bit rate option 9: 12165.12 Mbit/s, 64B/66B line coding (24 x 491.52 x 66/64 Mbit/s)

It is mandatory that each REC and RE support at least one of the above cited CPRI line bit rates.

All CPRI line bit rates have been chosen in such a way that the basic UMTS chip rate of 3.84 Mbit/s can be recovered in a cost-efficient way from the line bit rate taking into account the line coding schemes as defined in Section 4.2.5. For example, the 1228.8 Mbit/s correspond to an encoder rate of 122.88 MHz for the 8B/10B encoder and a subsequent frequency division by a factor of 32 provides the basic UMTS chip rate.

4.2.2. Physical Layer Modes

CPRI is specified for several applications with different interface line bit rates and REC to RE ranges. Table 2 defines several CPRI physical layer modes:

Table 2: CPRI physical layer modes

Line bit rate	Electrical	Optical	
		Short range	Long range
614.4 Mbit/s	E.6	OS.6	OL.6
1228.8 Mbit/s	E.12	OS.12	OL.12
2457.6 Mbit/s	E.24	OS.24	OL.24
3072.0 Mbit/s	E.30	OS.30	OL.30
4915.2 Mbit/s	E.48	OS.48	OL.48
6144.0 Mbit/s	E.60	OS.60	OL.60
8110.08 Mbit/s[3]	E.79	N.A.[3]	N.A.[3]
9830.4 Mbit/s	E.96	OS.96	OL.96
10137.6 Mbit/s	E.99	OS.99	OL.99
12165.12 Mbit/s	E.119	OS.119	OL.119

For each of those CPRI "modes" the layer one shall fulfil the requirements as specified in Section 7.1.5 (clock stability and noise) and Sections 7.1.8.2 and 7.1.8.3 (BER < 10^{-12}).

Four electrical variants are recommended for CPRI usage, denoted HV (high voltage), LV (low voltage), LV-II (low voltage II) and LV-III (low voltage III) in Figure 6A below. The HV variant is guided by IEEE 802.3 [22], clause 39 (1000base-CX) but with 100 ohm impedance. The LV variant is guided by IEEE 802.3 [22] clause 47 (XAUI) but with lower bit rate. The LV-II variant is guided by OIF-CEI-02.0, clause 7, but with lower bit rate. The LV-III variant is guided by IEEE 802.3 [22], clause 72.7 and 72.8 (10GBase-KR). See annex 6.2 for more details on the adaptation to CPRI line bit rates and applications.

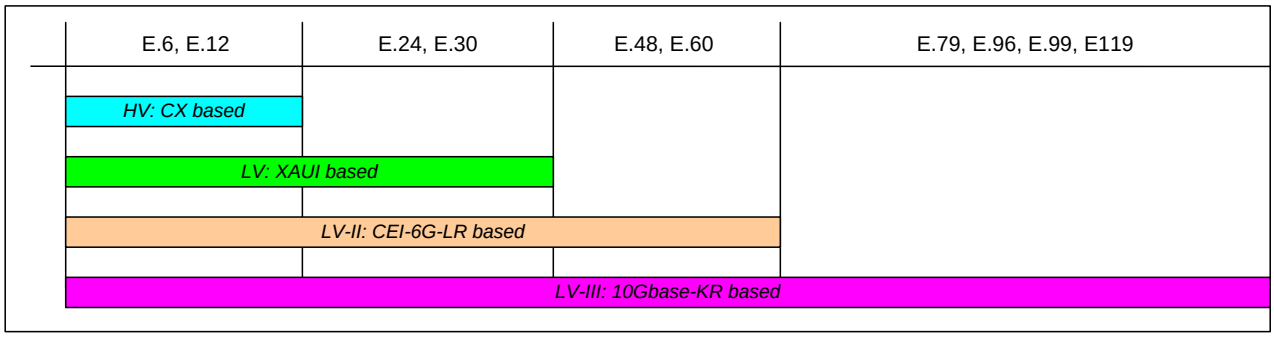


Figure 6A: HV (high voltage), LV (low voltage), LV-II and LV-III electrical layer 1 usage

It is recommended to reuse optical transceivers from the following High Speed Serial Link standards:

- Gigabit Ethernet: Standard IEEE 802.3 [22] clause 38 (1000BASE-SX/LX)
- 10 Gigabit Ethernet: Standard IEEE 802.3 [22] clause 53 (10GBASE-LX4)
- Fibre channel (FC-PI) – Standard ISO/IEC 14165-115 [3]
- Fibre channel (FC-PI-4) – INCITS (ANSI) Revision 8, T11/08-138v1 [18]
- Infiniband Volume 2 Rel 1.1 (November 2002) [6]

[3] Line bit rate option 7A (8110.08 Mbps) has exactly the same information bit rate as option 7 but with a different line coding scheme and lower line bit rate. It is intended to be used for intra-REC and/or intra-RE electrical interface only.

- 10 Gigabit Ethernet: Standard IEEE 802.3 [22], Clause 52(10GBASE-S/L/E)
- 40 Gigabit Ethernet: Standard IEEE 802.3 [22], Clause 87 (40GBASE-LR4)
- Fibre channel (FC-PI-5) – INCITS (ANSI) Revision 6.10, T11/11-011v0 [28]

If Wavelength Division Multiplexed (WDM) optical transceivers are used; each WDM lane may be used as an independent CPRI link.

The specification does not preclude the usage of any other technique that is proven to reach the same BER performance (BER < 10^{-12}) and clock stability for the dedicated CPRI application.

CPRI clock tolerance is driven by 3GPP requirements (see 3GPP TS 25.104 [8]), which fully permits the usage of existing high speed serial link standards.

4.2.3. Electrical Interface

4.2.3.1. Electrical Cabling

No specific cabling is recommended by CPRI.

The cable performance shall be such that transmitter and receiver performance requirements in section 7.1 are fulfilled. See also annex 6.2 for explicit recommendations on electrical characteristics.

4.2.3.2. Electrical Connectors

CPRI electrical implementation may use connector solutions that are described and defined in ISO/IEC 14165-115 (Fibre channel FC-PI) [3], INCITS Fibre channel FC-PI-4 [18] or IEEE 802.3 [22].

These solutions are known to achieve the performance required in section 7.1. See also annex 6.2 for explicit recommendations on electrical characteristics.

4.2.4. Optical Interface

4.2.4.1. Optical Cabling

The cable performance shall be such that transmitter and receiver performance requirements in section 7.1 are fulfilled. The fiber cables recommended for CPRI are:

- IEC 60793-2-10:2002.Type A1a (50/125 µm multimode) [4]
- IEC 60793-2-10:2002.Type A1b (62.5/125 µm multimode) [4]
- IEC 60793-2-50:2002.Type B1 (10/125 µm single-mode) [5]

The exception characteristic as specified in IEEE 802.3 [22] Table 38-12 and IEEE 802.3 [22] Table 53-14 as well as INCITS Fibre channel FC-PI-4 [18] Table 6 and Table 10 may be taken into account.

4.2.4.2. Optical Connectors

CPRI optical implementation may use connector solutions that are described and defined in ISO/IEC 14165-115 [3] (Fibre channel FC-PI), INCITS Fibre channel FC-PI-4 [18] or IEEE 802.3 [22].

These solutions are known to achieve the performance requirements in section 7.1. A high flexibility in the choice of connector and transceiver can be achieved by adopting the SFP [19], SFP+ [20], [21] and QSFP+ [26], [27] building practice.

4.2.5. Line Coding

For CPRI line bit rate options 1, 2, 3, 4, 5, 6 and 7 the 8B/10B line coding shall be used for serial transmission according to IEEE 802.3 [22], clause 36.

For CPRI line bit rate option 7A, 8 and 9 the 64B/66B line coding shall be used for serial transmission according to IEEE 802.3 [22], clause 49.

4.2.6. Bit Error Correction/Detection

The physical layer is designed in such a way that a very low bit error ratio can be achieved without expensive forward error correction schemes (see requirement R-27). Therefore, no general bit error correction is applied at layer 1. Some layer 1 control bits have their own protection, see chapter 4.2.7.6.2.

For 8B/10B line coding the RE and the REC shall support detection of 8B/10B code violations. Link failures shall be detected by means of 8B/10B code violations.

For 64B/66B line coding the RE and the REC shall support detection of sync header violations. Link failures shall be detected by means of sync header violations.

4.2.7. Frame Structure

4.2.7.1. Basic Frame Structure

4.2.7.1.1. Framing Nomenclature

The length of a basic frame is 1 T_C = 1/fc = 1/3.84 MHz = 260.416667ns. A basic frame consists of 16 words with index W=0…15. The length T of the word depends on the CPRI line bit rate as shown in Table 3. Each bit within a word is addressed with the index B, where B=0 is the LSB and B=T-1 is the MSB. Each BYTE within a word is addressed with the index Y, where B=0 is LSB of Y=0, B=7 is MSB of Y=0, B=8 is LSB of Y=1, etc...

The first T_{CW} bits of the word with index W=0 are used for one control word. If T_{CW} is not equal to T, the remaining (T-T_{CW}) bits of the word with index W=0 are for real time vendor specific usage (according to section 7.1.4.4 real time vendor specific usage also includes U-plane IQ data transport).

For the notation #Z.X.Y please refer to Section 4.2.7.3.

Table 3: Length of control word

CPRI line bit rate [Mbit/s]	length of word [bit]	Length of control word [bit]	control word consisting of BYTES with index
614.4	T=8	T_{CW} = T	Z.X.0
1228.8	T=16		Z.X.0, Z.X.1
2457.6	T=32		Z.X.0, Z.X.1, Z.X.2, Z.X.3
3072.0	T=40		Z.X.0, Z.X.1, Z.X.2, Z.X.3, Z.X.4
4915.2	T=64		Z.X.0, Z.X.1, Z.X.2, Z.X.3, Z.X.4, Z.X.5, Z.X.6, Z.X.7
6144.0	T=80		Z.X.0, Z.X.1, Z.X.2, Z.X.3, Z.X.4, Z.X.5, Z.X.6, Z.X.7, Z.X.8, Z.X.9
8110.08, 9830.4	T=128		Z.X.0, Z.X.1, Z.X.2, Z.X.3, Z.X.4, Z.X.5, Z.X.6, Z.X.7, Z.X.8, Z.X.9, Z.X.10, Z.X.11, Z.X.12, Z.X.13, Z.X.14, Z.X.15
10137.6	T=160	T_{CW} = 128	Z.X.0, Z.X.1, Z.X.2, Z.X.3, Z.X.4, Z.X.5, Z.X.6, Z.X.7, Z.X.8, Z.X.9, Z.X.10, Z.X.11, Z.X.12, Z.X.13, Z.X.14, Z.X.15
12165.12	T=192		

The remaining words (W=1…15), 15/16 of the basic frame, are dedicated to the U-plane IQ data transport (IQ data block).

4.2.7.1.2. Transmission Sequence and Scrambling

The control BYTES of one basic frame are always transmitted first. The basic frame structure is shown in Figure 7 to Figure 9 for different CPRI line bit rates. The generic basic frame structure is shown in Figures 9A and 9B for two different cases of T_{CW}.

For 8B/10B line coding:

The bit assignment within a BYTE is aligned with IEEE 802.3 [22], namely bit 7 (MSB) = H to bit 0 (LSB) = A. The physical transmission sequence of the encoded data is defined by IEEE 802.3 [22]. The transmission sequence of the BYTES is indicated on the right hand side of Figure 7 to Figure 9B with one ball representing a BYTE. After 8B/10B encoding the 10bit code-groups ("abcdei fghj") are transmitted as serial data stream with bit "a" first.

If the protocol version BYTE #Z.2.0 is set to 2 all data shall be scrambled before 8B/10B line coding by a side-stream scrambler except for control BYTES #Z.X.Y with index Y≤1 of subchannel Ns=0 and subchannel Ns=2. Any seed – including zero – is allowed (see Annex 6.5 for more details on the scrambling mechanism).

A module being capable of supporting scrambling (according to annex 6.5) with any seed is defined to be a module supporting both protocol versions, #Z.2.0=2 and #Z.2.0=1. When transmitting (respectively receiving) with protocol version #Z.2.0=1 scrambling (respectively descrambling) shall be switched off, which can be achieved by setting the seed to zero. The protocol version is used in the start-up sequence as specified in section 4.5.

For 64B/66B line coding:

The coding is based on a block size of 64 bits. The hyperframe start shall be aligned with the beginning of the 64 bits block. The first bit of the CPRI basic frame (W=0, B=0) shall be mapped on the first bit of the 64 bits block. The physical transmission sequence of the encoded data is defined by IEEE 802.3 [22] clause 49. After 64B/66B encoding, the 66 bits transmit block "TxB<0..65>" is transmitted as serial data stream with bit TxB<0> (the first bit of sync header) first.

The scrambling of the payload is performed by the 64B/66B scrambler as defined by IEEE 802.3 [22] clause 49 and the scrambling as defined in Section 6.5 is bypassed.

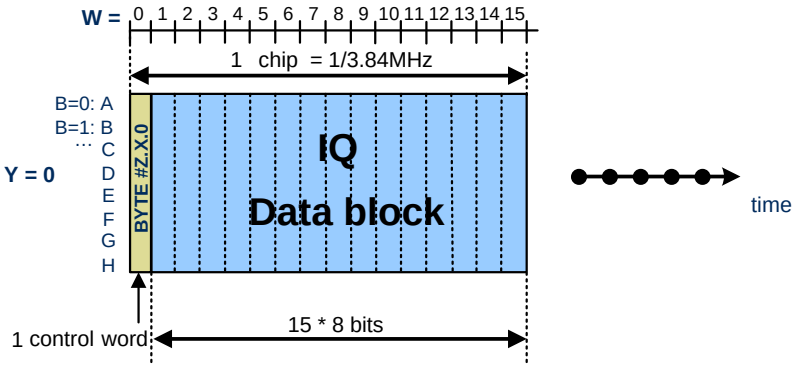


Figure 7: Basic frame structure for 614.4 Mbit/s CPRI line bit rate

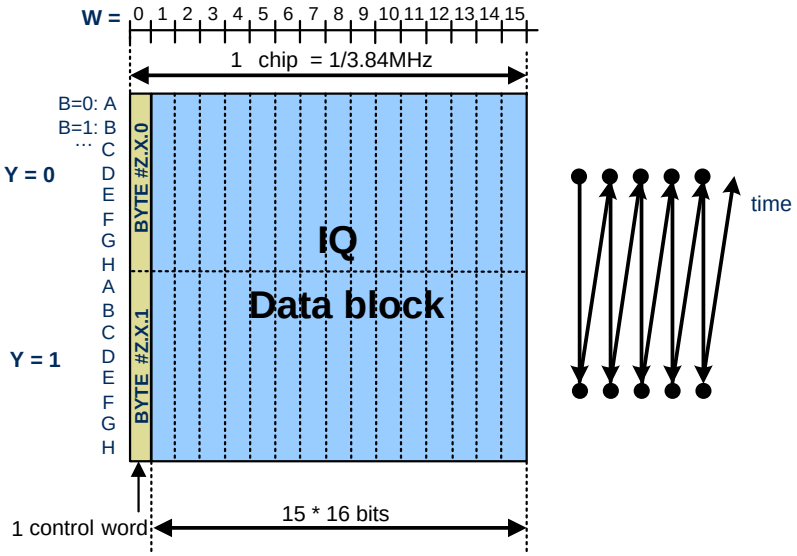


Figure 8: Basic frame structure for 1228.8 Mbit/s CPRI line bit rate

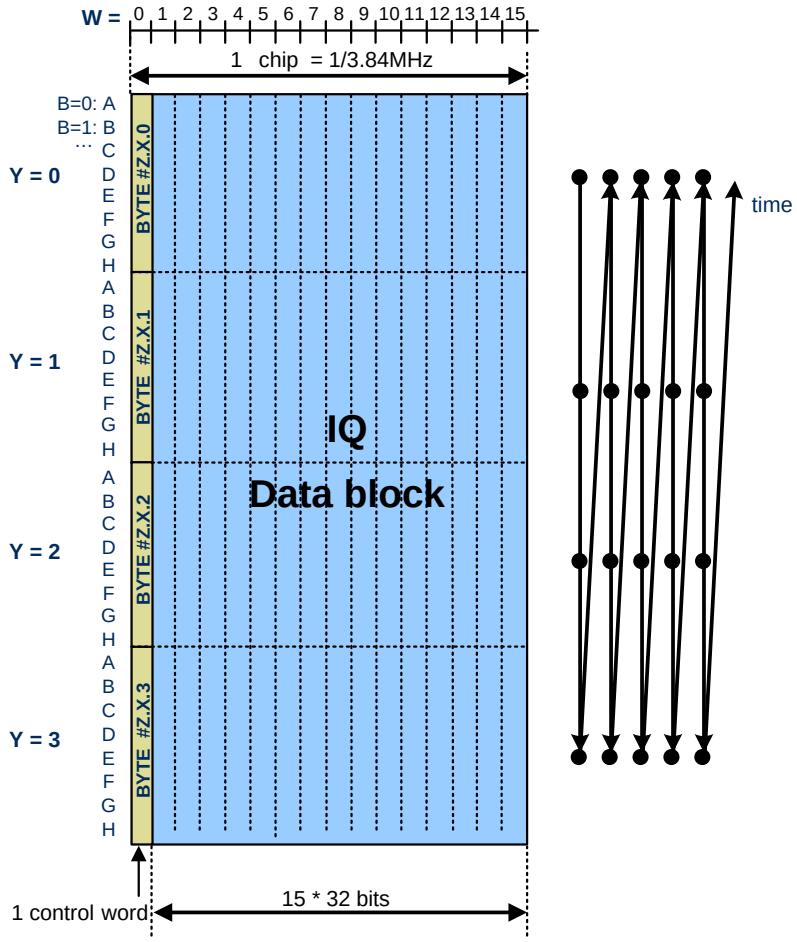


Figure 9: Basic frame structure for 2457.6 Mbit/s CPRI line bit rate

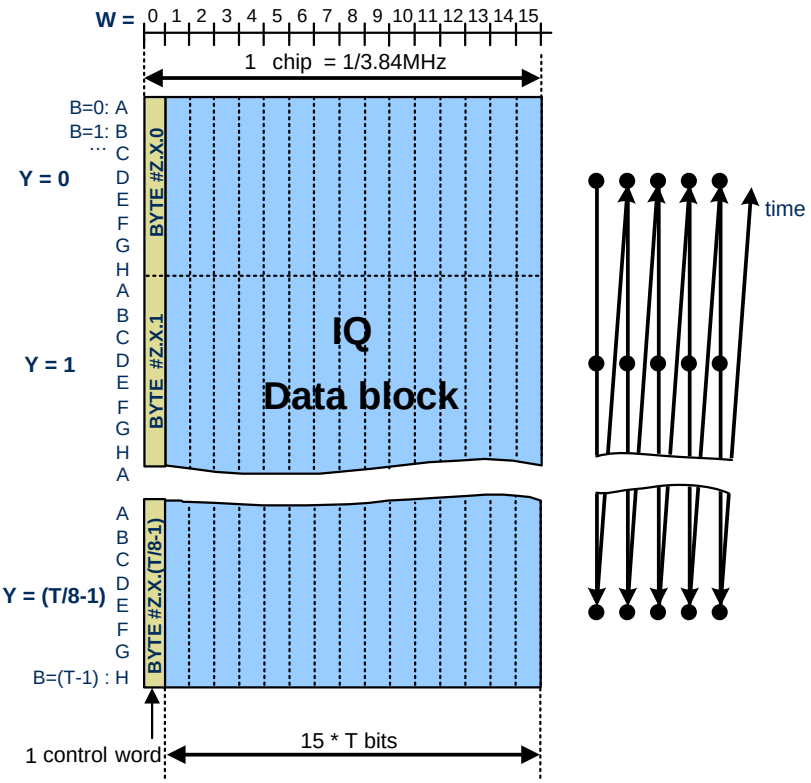


Figure 9A: Generic basic frame structure for T_{CW} = T
(T_{CW} and T are defined in Table 3)

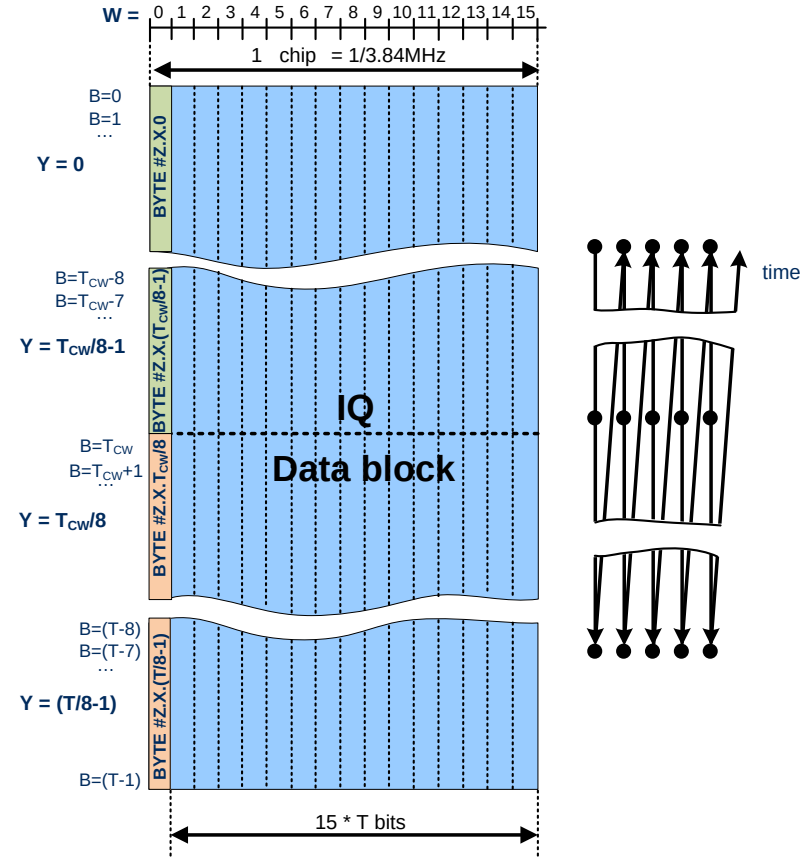


Figure 9B: Generic basic frame structure for cases where T_{CW} is not equal to T

4.2.7.2. Mapping of IQ data

4.2.7.2.1. IQ Sample Widths and IQ Formats

The required sample width of the user-plane IQ data depends on the application layer. This specification provides a universal mapping scheme in order to implement any of the required sample widths depending on the application layer. The option list for I and Q sample widths M and M' can be found in Table 4. Mixed sample widths within one basic frame are not described in detail but are allowed if required.

Table 4: Option list for I and Q sample width ranges

Direction of link	**Symbol for sample width**	**Range [bits]**
Downlink	M	8, 9, 10, …, 20
Uplink	M'	4, 5, 6, …, 20

In the standard case, one IQ sample consists of one I sample and one equal-sized Q sample (width M for downlink and M' for uplink).

In the mantissa-exponent uplink case, one IQ sample consists of:

- one I sample mantissa (width L),
- one equal-sized Q sample mantissa (width L),
- and one shared exponent (width 2N).

In case of mantissa-exponent uplink IQ data the width L of the I sample mantissa as well as of the Q sample mantissa is given by the following equation:

$$L = M' - N$$

where the values of M' and N are vendor specific, with the valid range of M' given by Table 4, and N being within the following range:

$$0 \le N \le M'-2$$

The width of the shared exponent shall be 2N.

The mantissa-exponent uplink IQ format is recommended for GSM uplink IQ data.

The interpretation of the mantissa-exponent uplink IQ format shall be as follows:

I_0, $I_{1,\ldots,}$ I_{L-1} and Q_0, Q_1,…, Q_{L-1} represent the I and Q sample mantissa respectively, while E_0, E_1,..., E_{2N-1} represent the shared exponent as unsigned integer. The mantissa is represented in 2's-complement where the I_{L-1} and Q_{L-1} bits are the sign bits. The actual I- and Q-value can be reconstructed from the sample format (being illustrated in Figure 12A) as follows:

$$I = \left(\left(\sum_{i=0}^{L-2} 2^i \cdot I_i \right) - 2^{L-1} \cdot I_{L-1} \right) \cdot 2^{EXP}$$

$$Q = \left(\left(\sum_{i=0}^{L-2} 2^i \cdot Q_i \right) - 2^{L-1} \cdot Q_{L-1} \right) \cdot 2^{EXP}$$

for N>0 the EXP is calculated as follows:

$$EXP = \sum_{j=0}^{2N-1} (2^j \cdot E_j)$$

For N=0 the value of EXP is equal to 0.

4.2.7.2.2. Mapping of IQ Samples within one **AxC Container**

An **AxC Container** is a sub-part of the IQ data block of a basic frame.

- For UTRA-FDD, an **AxC Container** contains exactly *n* IQ samples from the same AxC, where *n* is the oversampling ratio with respect to the chip rate f_C = 3.84MHz. The oversampling ratio *n* is defined in Table 5 and Table 5A. For UTRA-FDD the sampling rate is given by $f_S = n \cdot f_C$.
- For WiMAX, an **AxC Container** contains IQ sample bits and/or stuffing bits. One of the IQ mapping methods 1, 2 or 3, as specified in the following sections, shall apply per WiMAX AxC. For WiMAX the sampling rate f_S can be derived from the definitions given in [11].
- For E-UTRA, an **AxC Container** contains IQ sample bits from the same AxC and/or stuffing bits. The E-UTRA IQ samples shall be mapped to the **AxC Container** according to Mapping method 1 (section 4.2.7.2.5) or Mapping method 3 (section 4.2.7.2.7). For E-UTRA the typical sampling rates f_S can be derived from the 3GPP TS 36.104 [14] and 36.211 [16] as described in Annex 6.4.
- For GSM, an **AxC Container** contains IQ sample bits from the same AxC and/or stuffing bits. The GSM IQ samples shall be mapped to the **AxC Container** according to Mapping method 1 (section 4.2.7.2.5) or Mapping method 3 (section 4.2.7.2.7). For GSM, the sampling rate is assumed to be either a multiple of the GSM symbol rate or an integer multiple or sub-multiple of the UTRA-FDD chip rate (3.84MHz) as described in Annex 6.6.

The size of one **AxC Container** N_{AxC} shall be an even number of bits.

In the standard case (Figures 10 to 12) IQ sample(s) shall be sent in an **AxC Container** in the following way:

- in chronological order and consecutively,
- from LSB (I_0, Q_0) to MSB (I_{M-1}, Q_{M-1}) or ($I_{M'-1}$, $Q_{M'-1}$),
- I and Q samples being interleaved.

In the mantissa-exponent uplink IQ format case (Figure 12A) IQ sample(s) shall be sent in an **AxC Container** in the following way:

- in chronological order and consecutively,
- from LSB (I_0, Q_0) to MSB (I_{L-1}, Q_{L-1}),
- I sample mantissa and Q sample mantissa being interleaved,
- followed by the shared exponent in one block (from LSB (E_0) to MSB (E_{2N-1})).

The option lists for uplink and downlink oversampling ratios *n* can be found in Table 5 and Table 5A, respectively. The oversampling ratios of uplink and downlink may be selected independently.

Table 5: Option list for UTRA FDD UL oversampling ratios *n* with respect to f_C

	Opt. 1	**Opt. 2**
UL Oversampling Ratio *n*	2	4
UL Symbols for IQ samples	I, Q, I', Q'	I, Q, I', Q', I'', Q'', I''', Q'''

Table 5A: Option list for UTRA FDD DL oversampling ratios *n* with respect to f_C

	Opt. 1	**Opt. 2**
DL Oversampling Ratio *n*	1	2
DL Symbols for IQ samples	I, Q	I, Q, I', Q'

The IQ sample widths and the oversampling ratios for downlink and uplink shall be decided on application layer per AxC. Figure 10 to Figure 12 show the IQ sample arrangement and the transmission order for uplink and downlink for the described oversampling options.

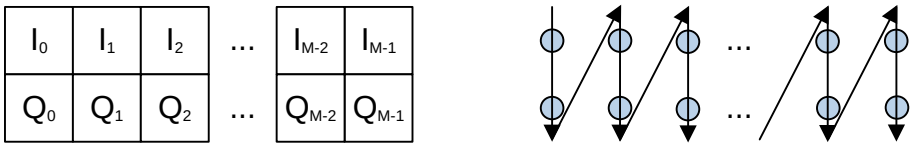


Figure 10: IQ samples within one AxC with oversampling ratio 1

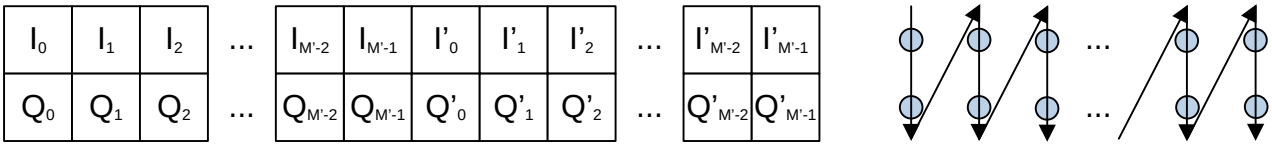


Figure 11: IQ samples within one AxC with oversampling ratio 2 (uplink direction shown; for the downlink direction M' shall be replaced by M)

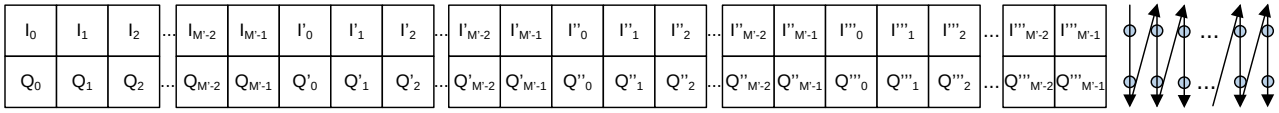


Figure 12: IQ samples within one uplink AxC with oversampling ratio 4

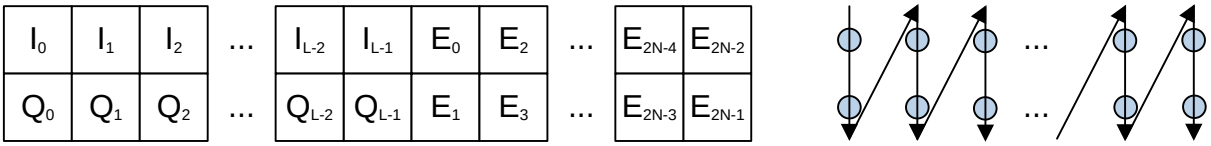


Figure 12A: IQ sample with mantissa-exponent uplink IQ data format

4.2.7.2.3. Mapping of **AxC Container** within one Basic Frame

The following mapping rules apply for both, uplink and downlink:

- Each **AxC Container** is sent as a block.
- Overlap of **AxC Containers** is not allowed.
- The position of each **AxC Container** in the IQ data block is decided by one of the following options:
  - Option 1 (packed position):

    Each **AxC Container** in a basic frame is sent consecutively (without any reserved bits in between) and in ascending order of AxC number.
  - Option 2 (flexible position):

For each **AxC Container**, the application shall decide at what address (W, B – for W>0) in the IQ data block the first bit of the **AxC Container** is positioned. The first bit of an **AxC Container** shall be positioned on an even bit position in the IQ data block (B shall be even).

- The bits not used by **AxC Containers** in the IQ data block in the basic frame shall be treated as reserved bits ("r").

Figure 13 illustrates these mapping rules for both mapping options.

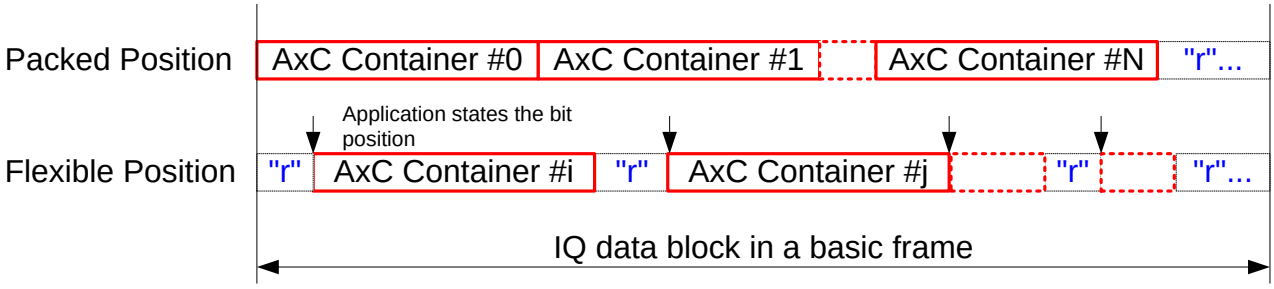


Figure 13: Example of **AxC Container** mapping in the IQ data block

4.2.7.2.4. Common properties of IQ mapping methods

Transmission of WiMAX/E-UTRA AxCs is organized in a consecutive flow of **AxC Container Blocks**, where each **AxC Container Block** has the duration of *K* basic frames. There are *S* IQ samples per WiMAX/E-UTRA AxC being carried in one **AxC Container Block**. The *S* IQ samples per WiMAX/E-UTRA AxC are mapped into the **AxC Container Block** in chronological order as shown in Figure 13A. Consecutive **AxC Container Blocks** construct a bit pipe. IQ samples with stuffing bits are arranged into the pipe as a continuous bit sequence. The synchronization between **AxC Container Blocks** and CPRI framing is specified in section 4.2.8.

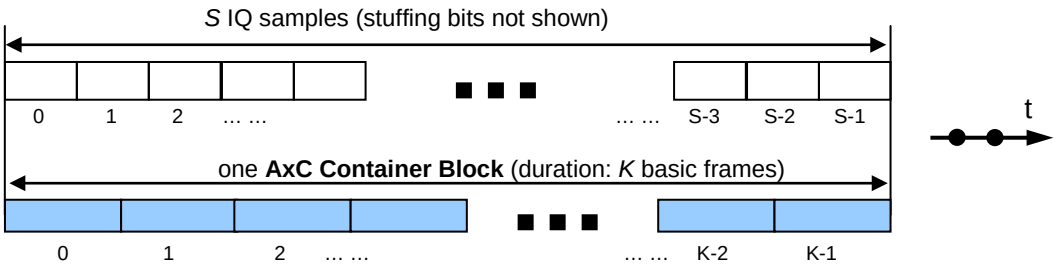


Figure 13A: Relation between *S* IQ samples and one **AxC Container Block**

S and *K* are non-zero integers. Different mapping methods provide different definitions for *S* and *K* as described in the sections 4.2.7.2.5, 4.2.7.2.6, and 4.2.7.2.7. For each AxC, the mapping method and the associated parameters (e.g. *S*, *K* values) are decided by the application layer in the REC[4]. The information is then sent to the RE(s) through the C&M channel.

4.2.7.2.5. Mapping method 1: IQ sample based

This mapping method is intended for dense packing of IQ data into the CPRI data flow (high bandwidth efficiency) and is optimized for low latency together with sample based processing of IQ data in the RE(s).

For this mapping method the size N_{AxC} of the **AxC Container** shall be chosen according to equation (3).

[4] An RE may not support all mapping methods. The REC shall take the capabilities of the RE into consideration for its decision.

$$N_{AxC} = 2 \cdot \mathrm{ceil}\left(\frac{M \cdot f_S}{f_C} \right) \quad (3)$$

The function “ceil” returns the smallest integer greater than or equal to the argument.

M is the width of I or Q sample for downlink as defined in Table 4. M’ shall be used instead of M for the uplink case. If no further information is given, the same rules shall be used for both, downlink and uplink.

For this mapping method the S and K shall satisfy equation (4).

$$\frac{S}{f_S} = \frac{K}{f_C} \quad (4)$$

S and *K* shall be calculated using equations (5) and (6).

$$K = \frac{\mathrm{LCM}(f_S, f_C)}{f_S}, \quad (5)$$

$$S = \frac{\mathrm{LCM}(f_S, f_C)}{f_C}, \quad (6)$$

where LCM means Least Common Multiple.

For this mapping method one **AxC Container Block** contains two parts, as shown in Figure 13B: The first part is filled with a number $N_{ST} = K \cdot N_{AxC} - 2 \cdot M \cdot S$ of stuffing bits; the second part is filled with *S* samples. The stuffing bits shall be vendor specific (“v”).

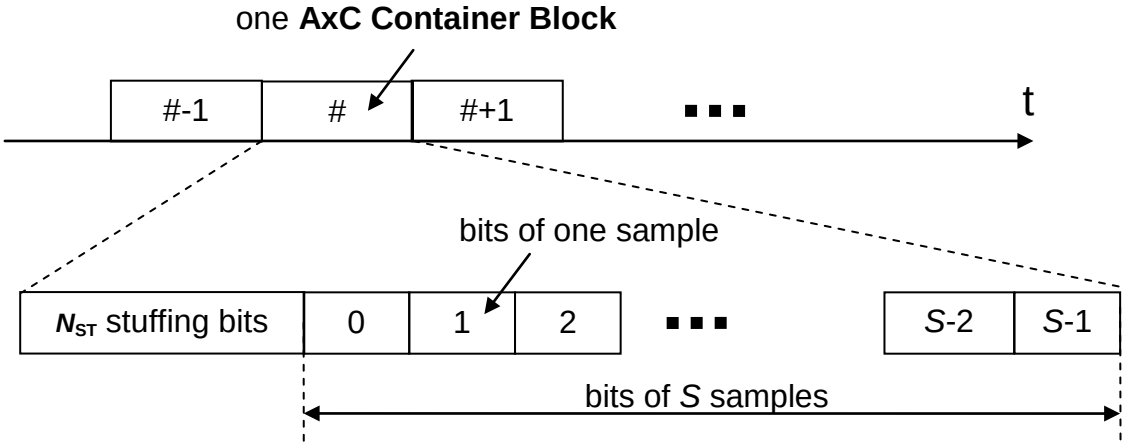


Figure 13B: IQ Sample based mapping in an **AxC Container Block**

4.2.7.2.6. Mapping method 2: WiMAX symbol based

This mapping method is intended for dense packing of IQ data into the CPRI data flow and is optimized for low latency together with WiMAX symbol based processing of IQ data in the RE(s).

The length K of the **AxC Container Block** shall be chosen equal to the WiMAX frame duration T_F, as described by the following equation (7).

$$K = T_F \cdot f_C \quad (7)$$

For all WiMAX frame durations T_F defined in [11], K is an integer. The **AxC Container Block** shall be aligned with the WiMAX frame.

For this mapping method one **AxC Container Block** contains two parts: The first part is filled with N_{SYM} **AxC Symbol Blocks**; the second part is filled with N_{S_FRM} stuffing bits[5]. N_{SYM} is the number of WiMAX symbols in one WiMAX frame as given by equation (8), where T_S is the duration of one symbol as defined in [13] section 8.3.2.2.

$$N_{\mathrm{SYM}} = \mathrm{floor}\left(\frac{\mathrm{T_F}}{\mathrm{T_S}}\right) \tag{8}$$

The function "floor" returns the greatest integer less than or equal to the argument.

In each **AxC Symbol Block**, there are also two parts: The first part is filled with N_{SAM} samples; the second part is filled with N_{S_SYM} stuffing bits. N_{SAM} is the number of samples (either with or without CP) during one WiMAX symbol.

The total number of S samples per **AxC Container Block** is given by equation (9):

$$S = N_{\mathrm{SYM}} \cdot N_{\mathrm{SAM}} \tag{9}.$$

All of these relations are illustrated in Figure 13C.

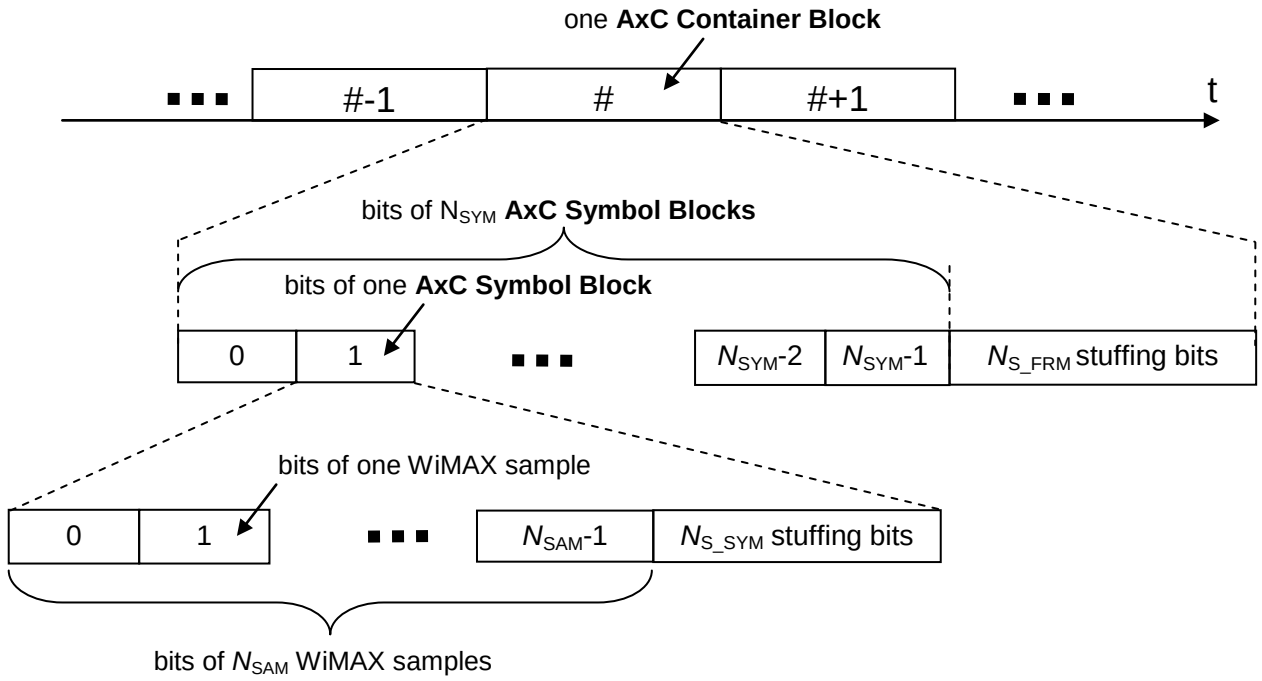


Figure 13C: Symbol based mapping in an **AxC Container Block**

For this mapping method the size N_{AxC} of the **AxC Container** shall be chosen according to inequality (10).

$$N_{\mathrm{AxC}} \geq 2 \cdot \mathrm{ceil}\left(\frac{\mathrm{M} \cdot S}{K}\right) \tag{10}$$

The number N_{S_SYM} of stuffing bits in one **AxC Symbol Block** and the number N_{S_FRM} of stuffing bits in one **AxC Container Block** are given by equations (11) and (12), respectively.

$$N_{\mathrm{S\_SYM}} = \mathrm{floor}\left(\frac{K \cdot N_{\mathrm{AxC}} - S \cdot 2 \cdot \mathrm{M}}{N_{\mathrm{SYM}}}\right) \tag{11}$$

[5] The N_{S_FRM} stuffing bits are required since the length of a WiMAX frame is in general not an integer multiple of symbol lengths.

$$N_{S\_FRM} = K \cdot N_{AxC} - S \cdot 2 \cdot M - N_{S\_SYM} \cdot N_{SYM} \quad (12)$$

4.2.7.2.7. Mapping method 3: Backward compatible

For this mapping method the size of the **AxC Container** N_{AxC} = 2·M shall be chosen with M being in the range as specified in Table 4.

This choice makes use of the **AxC Containers** which have been defined for UTRA-FDD in CPRI releases 1 and 2 for downlink. For uplink the same mapping method shall apply as for downlink. WiMAX/E-UTRA/GSM can be implemented as an application above a CPRI release 1 or 2 communication as shown in Figure 13D. One **AxC Container** contains exactly one sample (which could be a stuffing sample in case of WiMAX/E-UTRA/GSM). With this mapping method WiMAX/E-UTRA/GSM can easily be implemented in networking topologies where CPRI release 1 or 2 compatible REs already exist.

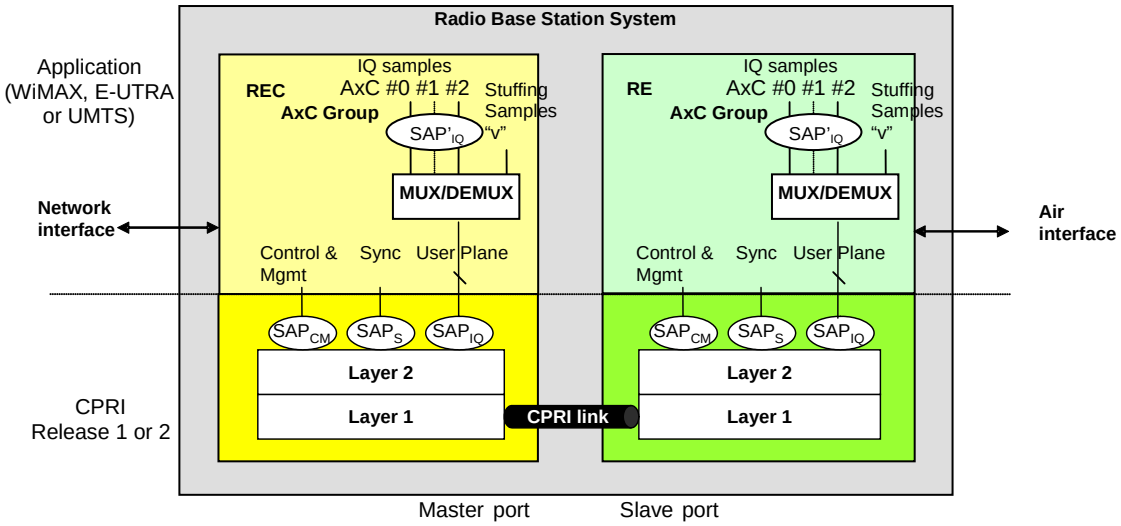


Figure 13D: Example of protocol stack based upon CPRI release 1 and 2

For this mapping method *S* and *K* shall be calculated by equations (5) and (6) as with IQ sample based mapping in section 4.2.7.2.5.

Multiplexed IQ samples of an **AxC Group** are carried in **AxC Container Groups** consisting of N_C **AxC Containers** per basic frame.

> The **AxC Group** contains N_A AxCs (AxC#0, AxC#1, …, AxC# N_A -1). However, it is not mandatory to handle AxCs with same features in an **AxC Group**, therefore N_A =1 is the basic configuration.

One **AxC Container Block** contains $N_A \cdot S$ samples.

N_C shall satisfy inequality (13).

$$N_C \geq \text{ceil}\left(\frac{N_A \cdot S}{K}\right) \quad (13)$$

N_C should be chosen by equation (14) in order to minimize the number of stuffing samples N_V that is defined in equation (15).

$$N_C = \text{ceil}\left(\frac{N_A \cdot S}{K}\right) \quad (14)$$

Within one **AxC Group** all samples shall have the same width M and all **AxC Containers** shall have the same size N_{AxC} = 2*M (Each IQ sample is stored in an **AxC Container** as specified in CPRI release 1 and 2).

One **AxC Container Block** contains $N_C \cdot K$ **AxC Containers**, which are indexed in chronological order from k=0 to $k=N_C*K-1$. The number N_V of stuffing samples per **AxC Container Block** is given by the equation (15):

$$N_V = N_C \cdot K - N_A \cdot S \quad (15)$$

For WiMAX, the values for S and K, as well as the recommended values for N_C and N_V are provided in Table 5B for the basic configuration with N_A =1 and N_A =2 and for the sampling rates f_S as specified in [11]. For E-UTRA, the corresponding values for the sampling rates listed in Annex 6.4 are shown in Table 5C. For GSM, the corresponding values for the sampling rates listed in Annex 6.6 are shown in Table 5D.

Table 5B: Recommended number N_V of stuffing samples for N_A =1 and N_A =2 (WiMAX)

f_S [MHz]	N_A	S	K	N_C	**$N_V = N_C \cdot K - N_A \cdot S$**
4	*1*	*25*	*24*	*2*	***23***
5.6	1	35	24	2	**13**
8	1	25	12	3	**11**
10	1	125	48	3	**19**
11.2	1	35	12	3	**1**
22.4	1	35	6	6	**1**
4	2	25	24	3	**22**
5.6	2	35	24	3	**2**
8	2	25	12	5	**10**
10	2	125	48	6	**38**
11.2	2	35	12	6	**2**
22.4	2	35	6	12	**2**

Table 5C: Recommended number N_V of stuffing samples for N_A =1 and N_A =2 (E-UTRA)

f_S [MHz]	N_A	S	K	N_C	**$N_V = N_C \cdot K - N_A \cdot S$**
1.92	1	1	2	1	**1**
3.84	1	1	1	1	**0**
7.68	1	2	1	2	**0**
15.36	1	4	1	4	**0**
23.04	1	6	1	6	**0**
30.72	1	8	1	8	**0**
1.92	2	1	2	1	**0**

Table 5D: Recommended number N_V of stuffing samples for *GSM*

f_S [kHz]	N_A	S	K	N_C	**$N_V = N_C \cdot K - N_A \cdot S$**
1625/6	1	325	4608	1	**4283**
1625/6	8	325	4608	1	**2008**
1625/6	14	325	4608	1	**58**
325	1	65	768	1	**703**
325	6	65	768	1	**378**
325	11	65	768	1	**53**
960	1	1	4	1	**3**
960	4	1	4	1	**0**
1625	1	325	768	1	**443**
1625	2	325	768	1	**118**
3250	1	325	384	1	**59**

In case of N_V >0 the position k_i of each stuffing sample i within the k=0 to $k=N_C*K-1$ AxC Containers is given by

$$k_i = \mathrm{floor}\left(\frac{i \cdot N_C \cdot K}{N_V}\right) \text{ ; for } i=0,1,\ldots, N_V - 1 \qquad (16)$$

The **AxC Containers** with index k_i are filled with stuffing samples which consist of vendor specific bits “v”. All remaining **AxC Containers** in the **AxC Container Block** are filled with samples of AxC#0, AxC#1, AxC#2,…, AxC#N_A-1 in chronological order. This mapping method is illustrated in Figure 13E.

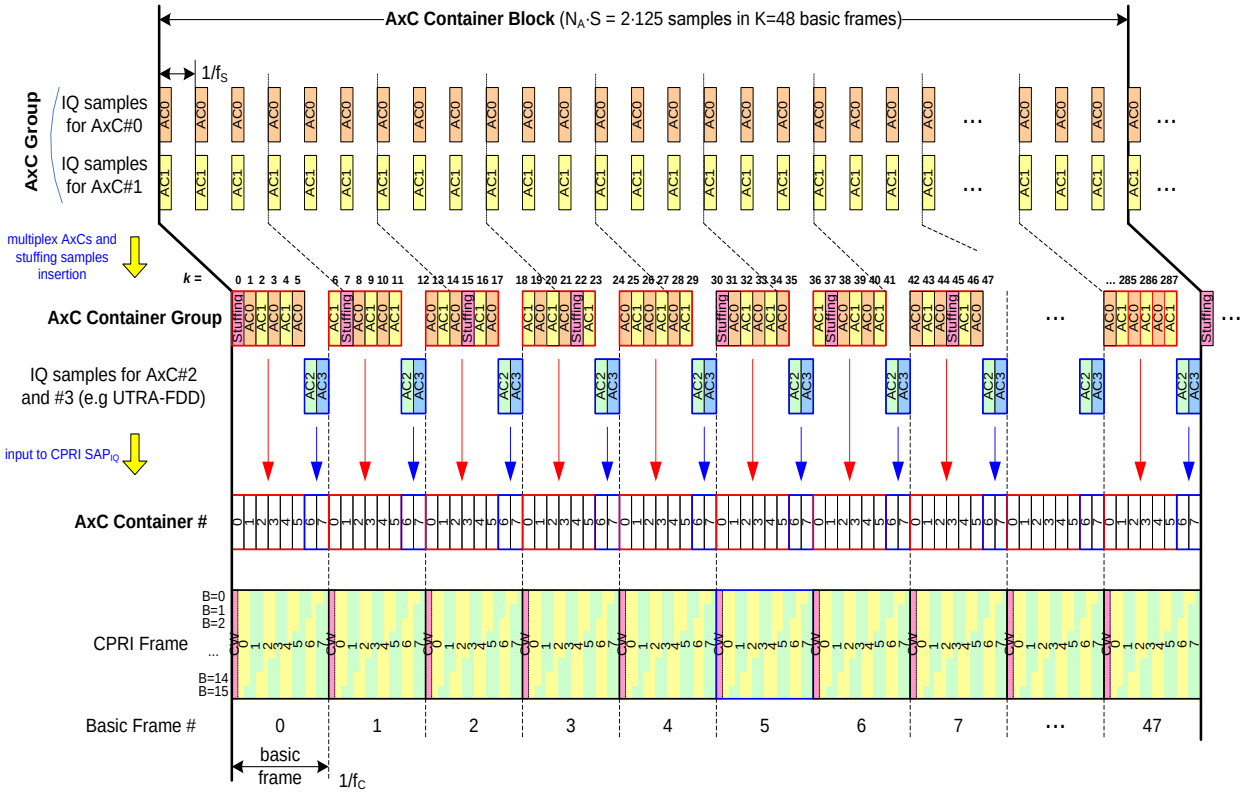


Figure 13E: Example of an **AxC Group** with N_A =2 (AxC#0, AxC#1) mapped into an **AxC Container Group** with N_C =6 **AxC Containers** per basic frame (**AxC Container #0** through **AxC Container #5**)

4.2.7.2.8. WiMAX/E-UTRA TDD and WiMAX/E-UTRA FDD

Both TDD and FDD have the same **AxC Container** definition and mapping rules as in the former sections. During the TDD sub-frame for uplink, there will be no IQ sample transfer in downlink, and the transmitter shall send stuffing bits “v”. During the TDD sub-frame for downlink, there will be no IQ sample transfer in uplink, and the transmitter shall send stuffing bits “v”.

TDD switching points in each WiMAX/E-UTRA frame shall be defined by the application layer in the REC, and be sent through the C&M channel to the RE(s).

4.2.7.3. Hyperframe Structure

The hyperframe structure is hierarchically embedded between the basic frame and the CRPI 10ms frame as shown in Figure 14.

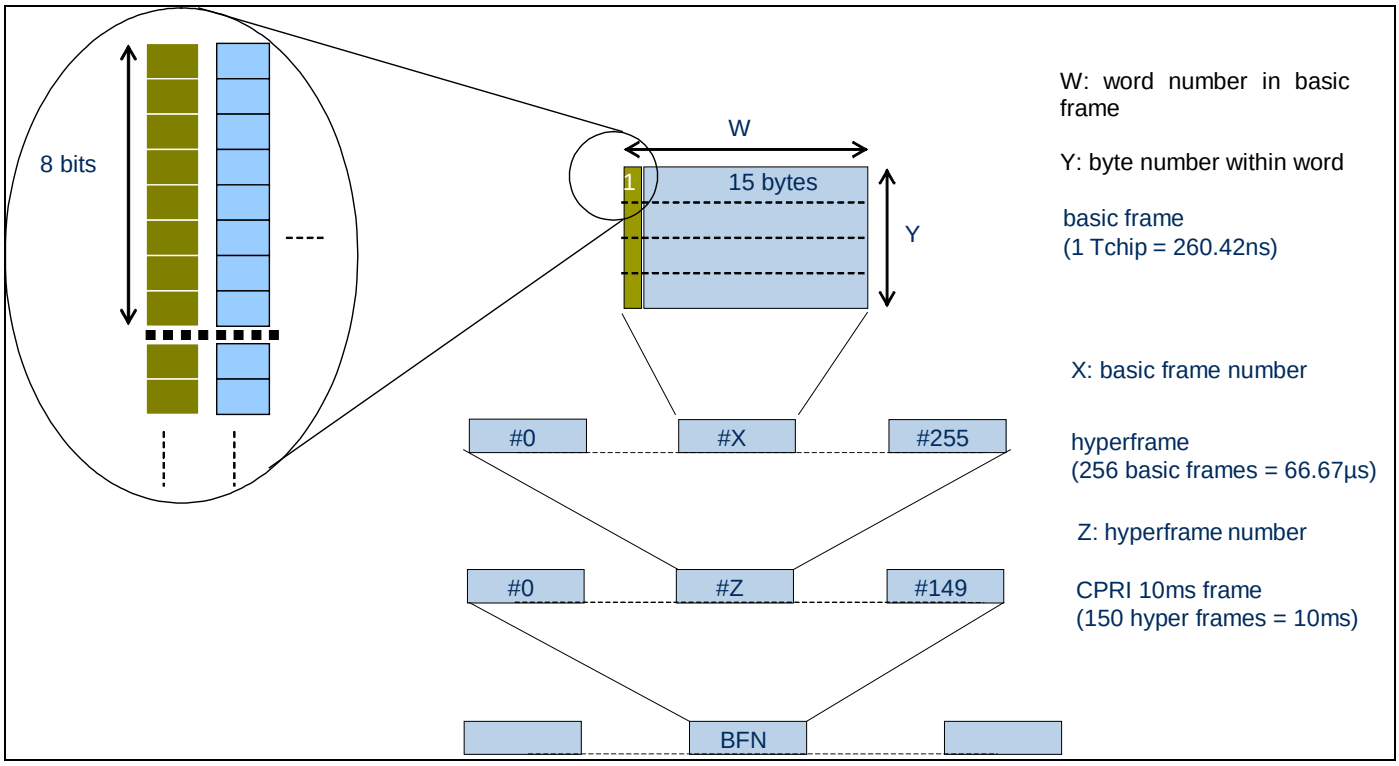


Figure 14: Illustration of the frame hierarchy and notation indices

Z is the hyperframe number, X is the basic frame number within a hyperframe, W is the word number within a basic frame and Y is the byte number within a word. The control word is defined as the first T_{CW} bits of the word with rank W=0. The value ranges of the indices are shown in Table 6:

Table 6: Value ranges of indices

CPRI line bit rate [Mbit/s]	**Z**	**X**	**W**	**Y**	**B**
614.4	0, 1, ..., 149	0, 1, …, 255	0, 1, …, 15	0	0, 1, … 7
1228.8				0, 1	0, 1, … 15
2457.6				0, 1, 2, 3	0, 1, … 31
3072.0				0, 1, 2, 3, 4	0, 1, … 39
4915.2				0, 1, 2, …, 7	0, 1, …, 63
6144.0				0, 1, 2, …, 9	0, 1, …, 79
8110.08, 9830.4				0, 1, 2, …, 15	0, 1, …, 127
10137.6				0, 1, 2, … , 19	0, 1, … , 159
12165.12				0, 1, 2, … , 23	0, 1, … , 191

4.2.7.4. Subchannel Definition

The 256 control words of a hyperframe are organized into 64 subchannels of 4 control words each. One subchannel contains 4 control words per hyperframe.

The index Ns of the subchannel ranges from 0 to 63. The index Xs of a control word within a subchannel has four possible values, namely 0, 1, 2 and 3. The index X of the control word within a hyperframe is given by X = Ns + 64*Xs.

The organization of the control words in subchannels is illustrated in Figure 15 and Figure 16.

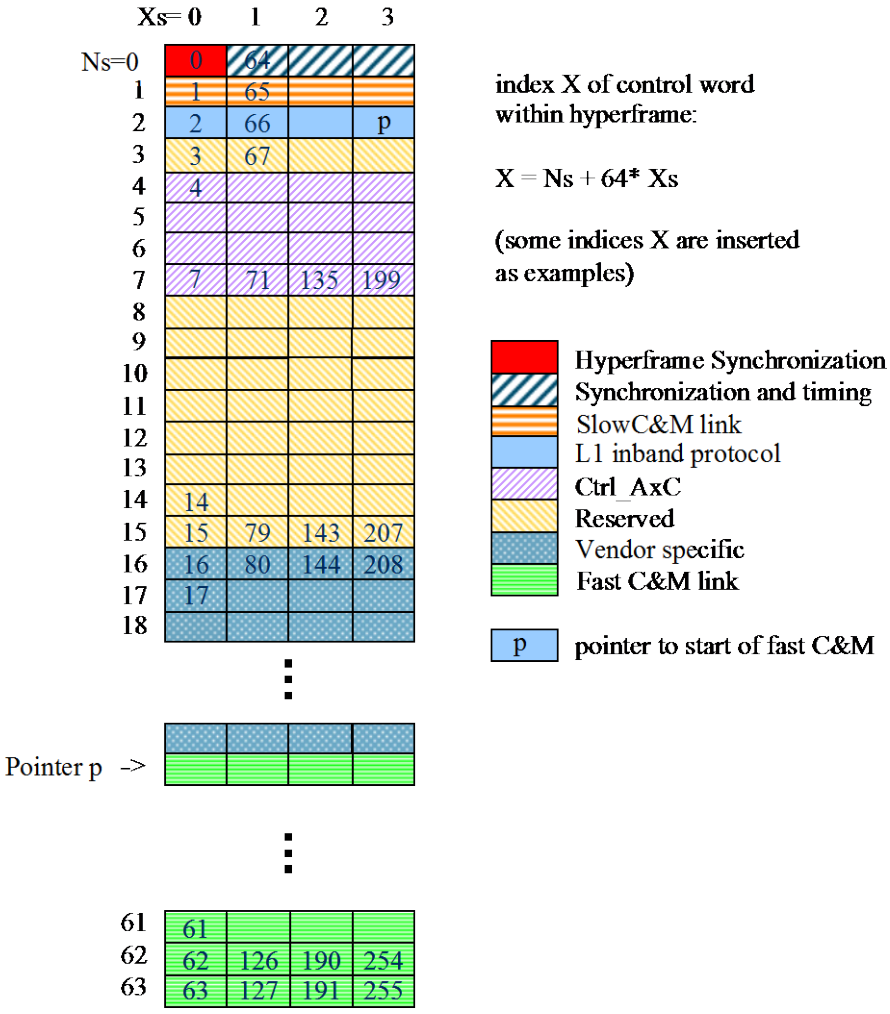


Figure 15: Illustration of subchannels within one hyperframe

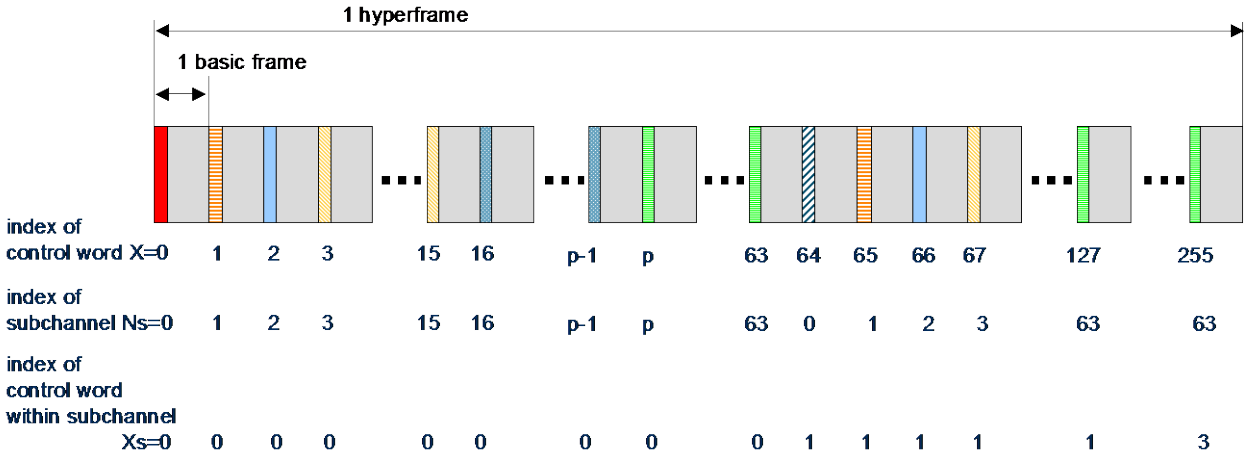


Figure 16: Illustration of control words and subchannels within one hyperframe

Table 7: Implementation of control words within one hyperframe for pointer p > 19

subchannel number Ns	purpose of subchannel	**Xs=0**	**Xs=1**	**Xs=2**	**Xs=3**
0	sync&timing	sync byte	HFN	BFN-low	BFN-high
1	slow C&M	slow C&M	slow C&M	slow C&M	slow C&M
2	L1 inband prot.	version	startup	L1-reset-LOS...	pointer p
3	reserved	reserved	reserved	reserved	reserved
4	Ctrl_AxC low Byte	Ctrl_AxC	Ctrl_AxC	Ctrl_AxC	Ctrl_AxC
5	Ctrl_AxC low Byte	Ctrl_AxC	Ctrl_AxC	Ctrl_AxC	Ctrl_AxC
6	Ctrl_AxC high Byte	Ctrl_AxC	Ctrl_AxC	Ctrl_AxC	Ctrl_AxC
7	Ctrl_AxC high Byte	Ctrl_AxC	Ctrl_AxC	Ctrl_AxC	Ctrl_AxC
8	reserved	reserved	reserved	reserved	reserved
...	...	...	...	...	...
15	reserved	reserved	reserved	reserved	reserved
16	vendor specific	vendor specific	vendor specific	vendor specific	vendor specific
...	...	...	...	...	...
p-1	vendor specific	vendor specific	vendor specific	vendor specific	vendor specific
pointer: p	fast C&M	fast C&M	fast C&M	fast C&M	fast C&M
...	...	...	...	...	...
63	fast C&M	fast C&M	fast C&M	fast C&M	fast C&M

For subchannel 0 the content of the control BYTES #Z.X.Y with index Y≥1 is reserved (“r”), except for the synchronization control word (Xs=0) where Table 9 applies for 8B/10B line coding and Table 9A for 64B/66B line coding. For subchannel 1 Table 11 applies. For subchannel 2 the content of the control BYTES #Z.X.Y with index Y≥1 is reserved (“r”). For subchannels 4 to 7 figure 23Z applies. For subchannels p to 63 table 12 applies.

4.2.7.5. Synchronization Data

The following control words listed in Table 8 are dedicated to layer 1 synchronization and timing. The support of the control words in Table 8, Table 9 and Table 9A is mandatory.

Table 8: Control words for layer 1 synchronization and timing

BYTE index	Function	content	comment
Z.0.0	Start of hyperframe (Sync Byte)	Special code K28.5 (8B/10B line coding, Table 9), 50h (64B/66B line coding, Table 9A)	First byte in a hyperframe
Z.64.0	HFN (Hyperframe number)	HFN=0…149, the first hyperframe in an UMTS radio frame has HFN=0. The exact HFN bit mapping is indicated in Figure 17.	CPRI 10ms frame synchronization, HFN and BFN are described in detail in sections 4.2.8 and 4.2.9.
Z.128.0 and Z.192.0	BFN (CPRI 10ms frame number; for UTRA FDD aligned with Node**B** **F**rame **N**umber)	#Z.128.0 (low byte) and b3-b0 of #Z.192.0 are BFN b7-b4 of #Z.192.0 are reserved (all “r”). The exact mapping is described in Figure 18.	

HFN is mapped within #Z.64.0 as defined in Figure 17.

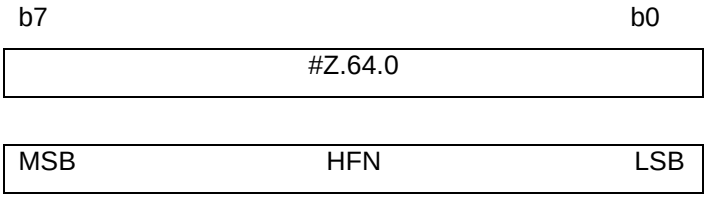


Figure 17: HFN mapping

BFN is mapped within #Z.128.0 and #Z.192.0 as defined in Figure 18. #Z.192.0 b7---b4 are reserved bits.

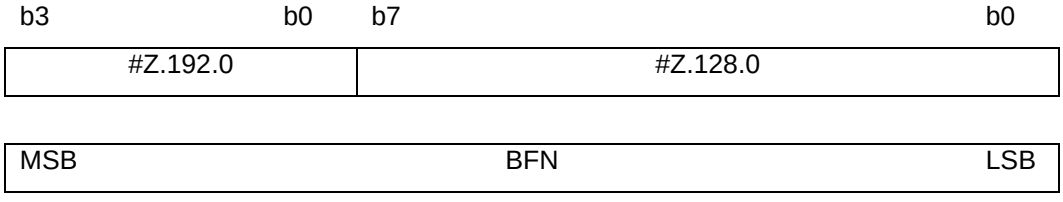


Figure 18: BFN mapping

Table 9: Synchronization control word for 8B/10B line coding

<table>
<tr><th colspan="3">CPRI line bit rate[Mbit/s]</th><th>614.4</th><th>1228.8</th><th>2457.6</th><th>3072.0</th><th>4915.2</th><th>6144.0</th><th>9830.4</th></tr>
<tr><td rowspan="17">Sync. Control Word</td><td>#Z.0.0</td><td>Sync. Byte</td><td>K28.5 (BCh)</td><td>K28.5 (BCh)</td><td>K28.5 (BCh)</td><td>K28.5 (BCh)</td><td>K28.5 (BCh)</td><td>K28.5 (BCh)</td><td>K28.5 (BCh)</td></tr>
<tr><td rowspan="2">#Z.0.1</td><td rowspan="15">Filling Bytes</td><td rowspan="15">N/A</td><td>D16.2 (50h)</td><td>D16.2 (50h)</td><td>D16.2 (50h)</td><td>D16.2 (50h)</td><td>D16.2 (50h)</td><td>D16.2 (50h)</td></tr>
<tr><td>D5.6 (C5h)</td><td>D5.6 (C5h)</td><td>D5.6 (C5h)</td><td>D5.6 (C5h)</td><td>D5.6 (C5h)</td><td>D5.6 (C5h)</td></tr>
<tr><td>#Z.0.2</td><td rowspan="13">N/A</td><td>D16.2 (50h)</td><td rowspan="2">D16.2 (50h)</td><td rowspan="4">D16.2 (50h)</td><td rowspan="3">D16.2 (50h)</td><td rowspan="11">D16.2 (50h)</td></tr>
<tr><td>#Z.0.3</td><td rowspan="12">N/A</td></tr>
<tr><td>#Z.0.4</td><td rowspan="11">N/A</td></tr>
<tr><td>#Z.0.5</td><td rowspan="10">N/A</td></tr>
<tr><td>#Z.0.6</td><td rowspan="9">N/A</td></tr>
<tr><td>#Z.0.7</td><td rowspan="8">N/A</td></tr>
<tr><td>#Z.0.8</td><td rowspan="7">N/A</td></tr>
<tr><td>#Z.0.9</td><td rowspan="6">N/A</td></tr>
<tr><td>#Z.0.10</td><td rowspan="5">N/A</td></tr>
<tr><td>#Z.0.11</td><td rowspan="4">N/A</td></tr>
<tr><td>#Z.0.12</td><td rowspan="3">N/A</td></tr>
<tr><td>#Z.0.13</td><td rowspan="2">N/A</td></tr>
<tr><td>#Z.0.14</td><td>N/A</td></tr>
<tr><td>#Z.0.15</td><td>N/A</td></tr>
</table>

Remark:

The sequences K28.5+D5.6 and K28.5+D16.2 are defined in the 8B/10B standard as /I1/ and /I2/ ordered_sets (IDLE1 sequences with opposing disparity and IDLE2 sequences with preserving disparity) and are expected to be supported by commonly used SERDES devices.

According to Table 9, the transmitter may send either D16.2 or D5.6 as BYTE #Z.0.1. The receiver shall accept both D16.2 and D5.6.

Table 9A: Synchronization control word for 64B/66B line coding

Sync. Control Word	#Z.0.0	Sync Byte	50h
	#Z.0.1	Filling Bytes	50h
	…		
	#Z.0.6		
	#Z.0.7	Terminate Control Character	/T/
	#Z.0.8	Start Control Character	/S/
	#Z.0.9	Filling Bytes	50h
	…		
	#Z.0.15		

According to Table 9A (64B/66B line coding), the transmitter will use the Terminate Control Character /T/ and the Start Control Character /S/ to provide hyperframe synchronization information, see section 6.7.2 and 6.7.3 for more detailed information. The bytes in Table 9A are input to XGMII as shown in Figure 49-5 in IEEE 802.3 [22].

4.2.7.6. L1 Inband Protocol

Reserved bits in this section are marked with “r”. This means that a transmitter shall send 0’s for bits marked with “r”, and the receiver shall not interpret bits marked with “r” (transmit: r = 0, receiver: r = don’t care).

The control BYTES listed in Table 10 are dedicated to L1 inband protocol.

Table 10: Control BYTES for L1 inband protocol

BYTE index	**function**	**content**	**comment**
Z.2.0	Protocol version	“0000 0001” or “0000 0010”	This document refers to protocol version 1 and 2
Z.66.0	Start-up	“rrrr rCCC” b2-b0 HDLC bit rate: 000: no HDLC 001: 240kbit/s HDLC 010: 480kbit/s HDLC 011: 960kbit/s HDLC (for line bit rates ≥ 1228.8Mbit/s) 100: 1920kbit/s HDLC (for line bit rates ≥ 2457.6Mbit/s) 101: 2400kbit/s HDLC (for line bit rates ≥ 3072.0Mbit/s) 110: Highest possible HDLC bit rate (for line bit rates > 3072.0Mbit/s)	Enables the HDLC link to be established

		111: HDLC bit rate negotiated on higher layer, see section 4.5.3.4. For an overview refer to Table 11 b7-b3: reserved (all “r”)	
Z.130.0	L1 SDI, RAI, Reset, LOS, LOF	“rrrF LSAR” b0: Reset 0: no reset 1: reset DL: reset request UL: reset acknowledge b1: RAI b2: SDI b3: LOS b4: LOF 0: alarm cleared 1: alarm set b7-b5: reserved (all “r”)	Basic layer 1 functions
Z.194.0	Pointer p	“rrPPPP PP” b5-b0: Pointer to subchannel number, where Ethernet link starts: 000000: p=0: no Ethernet channel 000001 … 010011: p=1…19 invalid (no Ethernet channel, not possible since other control words would be affected) 010100: … 111111: p=20…63: valid Ethernet channel, for bit rates refer to Table 12 b7-b6: reserved (all “r”)	Indicates the subchannel number Ns at which the control words for the Ethernet channel starts within a hyperframe.

4.2.7.6.1. Reset

Reset of the link is managed through start-up sequence definition (see Section 4.5). Reset of the RE is managed with the Reset bit in #Z.130.0. The reset notification can only be sent from a master port to a slave port. The reset acknowledgement can only be sent from a slave port to a master port. When the master wants to reset a slave, it shall set DL #Z.130.0 b0 for at least 10 hyperframes. On the reception of a valid reset notification, the slave shall set UL #Z.130.0 b0 at least 5 hyperframes on the same link.

When an RE receives a valid reset notification on any of its slave ports, it shall not only reset itself, but also forward reset notification on all its master ports by setting DL #Z.130.0 b0 for at least 10 hyperframes.

While in reset and if the link is still transmitting, the RE must set the SDI bit.

4.2.7.6.2. Protection of Signalling Bits

Signalling bits shall be protected by filtering over multiple hyperframes. The filtering shall be done by a majority decision of the 5 instances of one signalling bit derived from the 5 most recent hyperframes. The filtering guarantees that 2 consecutive erroneous receptions of instances of one signalling bit do not result in an erroneous interpretation.

This filtering requirement applies to the following signalling bit:

#Z.130.0, b0: “R” (Reset) in both DL and UL.

The filtering of the other inband protocol bits, i.e., #Z.66.0 (HDLC rate), #Z.194.0 (pointer to Ethernet channel), #Z.130.0 (layer 1 link maintenance) and #Z.2.0 (protocol version) shall be performed by the application layer (see also Section 4.2.10).

4.2.7.7. C&M Plane Data Channels

CPRI supports two different types of C&M channels, which shall be selected from the following option list:

- C&M Channel Option 1:Slow C&M Channel based on HDLC
- C&M Channel Option 2: Fast C&M Channel based on Ethernet

4.2.7.7.1. Slow C&M Channel

One option is to use a low rate HDLC channel for C&M data. The bit rate is defined by the 3 LSBs of the “start-up information” BYTE #Z.66.0 (see Table 11). The mapping of control BYTES to HDLC serial data is according to what is shown for the different configurations in Figure 19 to Figure 22.

Parameter T_{CW} used in Table 11 is defined in Table 3.

Table 11: Achievable HDLC bit rates in kbit/s

CPRI line bit rate [Mbit/s]	**#Z.66.0= rrrr r000**	**#Z.66.0= rrrr r001**	**#Z.66.0= rrrr r010**	**#Z.66.0= rrrr r011**	**#Z.66.0= rrrr r100**	**#Z.66.0= rrrr r101**	**#Z.66.0= rrrr r110**	**#Z.66.= rrrr r111**
614.4	no HDLC	240	480	invalid	invalid	invalid	invalid	See section 4.5.3.4 and section 4.5.3.5.
1228.8	no HDLC	240	480	960	invalid	invalid	invalid	
2457.6	no HDLC	240	480	960	1920	invalid	invalid	
3072.0	no HDLC	240	480	960	1920	2400	invalid	
4915.2	no HDLC	240	480	960	1920	2400	3840	
6144.0	no HDLC	240	480	960	1920	2400	4800	
8110.08, 9830.4, 10137.6, 12165.12	no HDLC	240	480	960	1920	2400	7680	
used control BYTE indices for the HDLC channel and their sequential order	no HDLC	Z.1.0 Z.129.0	Z.1.0 Z.65.0 Z.129.0 Z.193.0	Z.1.0 Z.1.1 Z.65.0 Z.65.1 Z.129.0 Z.129.1 Z.193.0 Z.193.1	Z.1.0 Z.1.1 Z.1.2 Z.1.3 Z.65.0 Z.65.1 Z.65.2 Z.65.3 Z.129.0 Z.129.1 Z.129.2 Z.129.3 Z.193.0 Z.193.1 Z.193.2 Z.193.3	Z.1.0 Z.1.1 Z.1.2 Z.1.3 Z.1.4 Z.65.0 Z.65.1 Z.65.2 Z.65.3 Z.65.4 Z.129.0 Z.129.1 Z.129.2 Z.129.3 Z.193.0 Z.193.1 Z.193.2 Z.193.3 Z.193.4	Z.1.0 Z.1.1 …. Z.1.(T_{CW}/8-1) Z.65.0 Z.65.1 ….. Z.65.(T_{CW}/8-1) Z.129.0 Z.129.1 …. Z.129.(T_{CW}/8-1) Z.193.0 Z.193.1 …. Z.193.(T_{CW}/8-1)	

Remark: In case of an invalid configuration no HDLC shall be used.

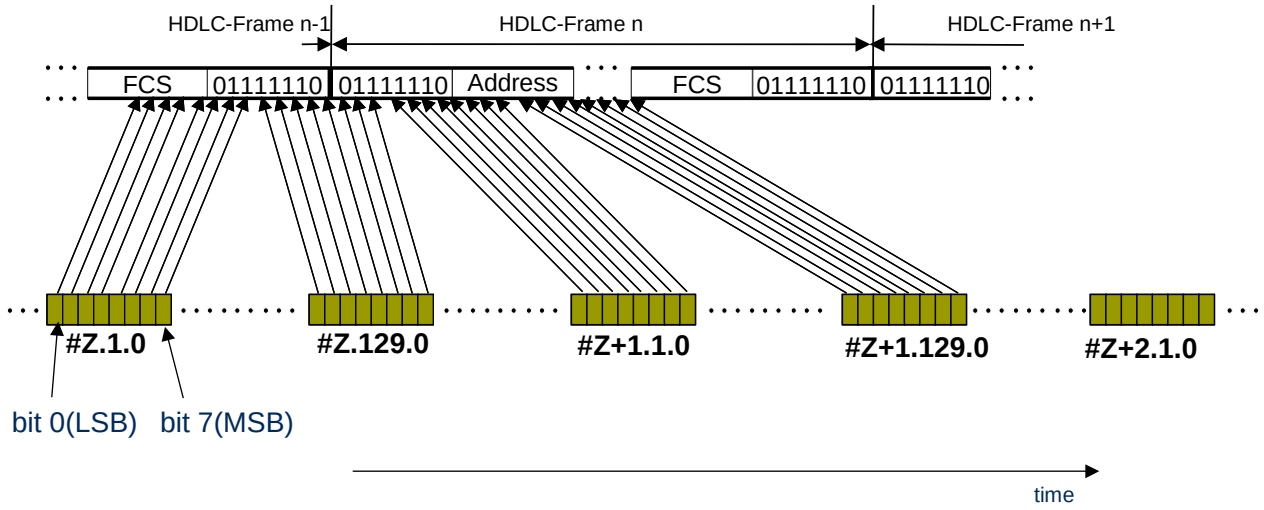


Figure 19: Mapping of control BYTES to HDLC serial data with 240kbit/s

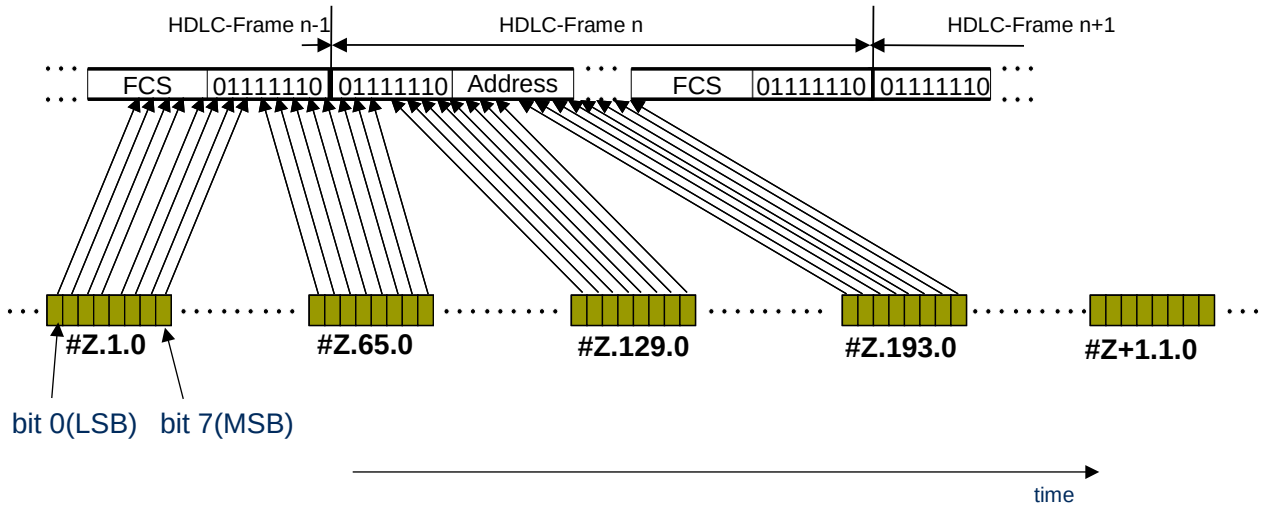


Figure 20: Mapping of control BYTES to HDLC serial data with 480kbit/s

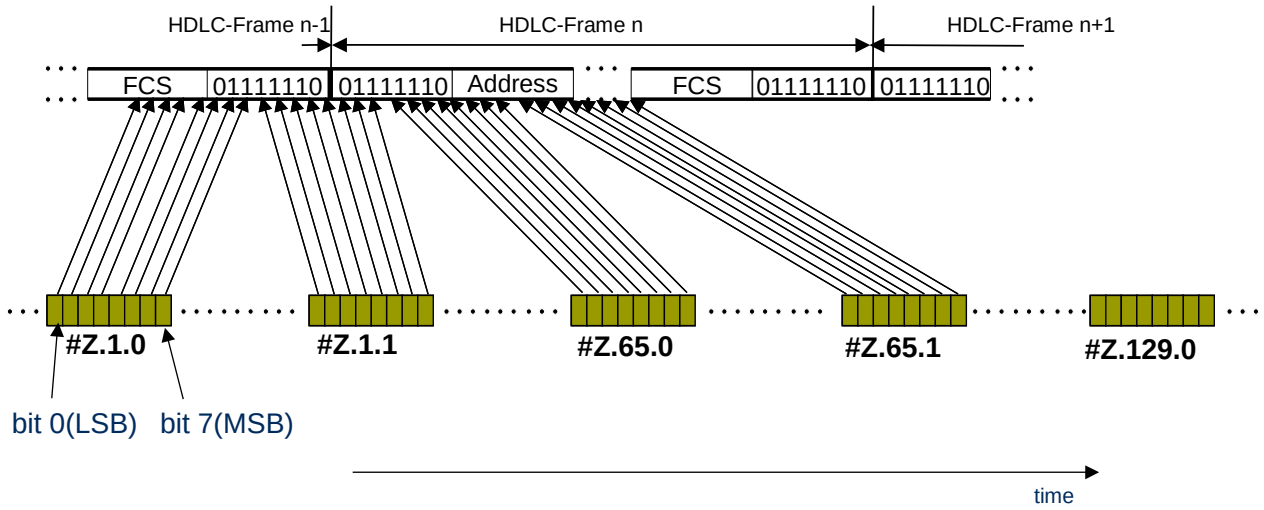


Figure 21: Mapping of control BYTES to HDLC serial data with 960kbit/s

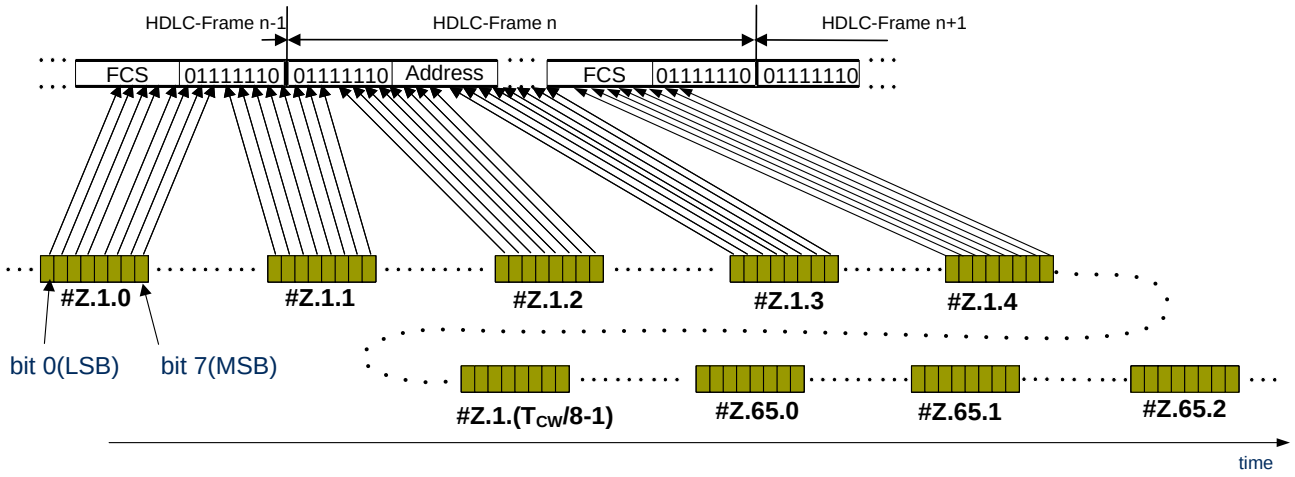


Figure 22: Mapping of control BYTES to HDLC serial data for #Z.66.0 = rrrr r110 (T_{CW} is defined in Table 3)

4.2.7.7.2. Fast C&M Channel

Another option is to use a high data rate Ethernet Channel which can be flexibly configured by the pointer in control BYTE #Z.194.0. The mapping of the Ethernet data follows the same principle as the HDLC channel (no byte alignment, LSB first).

The Ethernet bit rate is configured with the pointer in control BYTE #Z.194.0. In contrast to the HDLC link, the full control words shall always be used for the Ethernet channel. The achievable Ethernet bit rates are shown in Table 12.

Table 12: Achievable Ethernet bit rates

CPRI line bit rate [Mbit/s]	**length of control word [bit]**	**control word consisting of BYTES with index**	**minimum Ethernet bit rate [Mbit/s] (#Z.194.0=rr111111)**	**maximum Ethernet bit rate [Mbit/s] (#Z.194.0=rr010100)**
614.4	8	Z.X.0	0.48	21.12
1228.8	16	Z.X.0, Z.X.1	0.96	42.24
2457.6	32	Z.X.0, Z.X.1, Z.X.2, Z.X.3	1.92	84.48
3072.0	40	Z.X.0, Z.X.1, Z.X.2, Z.X.3, Z.X.4	2.4	105.6
4915.2	64	Z.X.0, Z.X.1, Z.X.2, Z.X.3, Z.X.4, Z.X.5, Z.X.6, Z.X.7	3.84	168.96
6144.0	80	Z.X.0, Z.X.1, Z.X.2, Z.X.3, Z.X.4, Z.X.5, Z.X.6, Z.X.7, Z.X.8, Z.X.9	4.8	211.2
8110.08, 9830.4, 10137.6, 12165.12	128	Z.X.0, Z.X.1, Z.X.2, Z.X.3, Z.X.4, Z.X.5, Z.X.6, Z.X.7, Z.X.8, Z.X.9, Z.X.10, Z.X.11, Z.X.12, Z.X.13, Z.X.14, Z.X.15	7.68	337.92

Packet detection, start and termination is based on SSD and ESD coding sequence as shown in Figure 23.

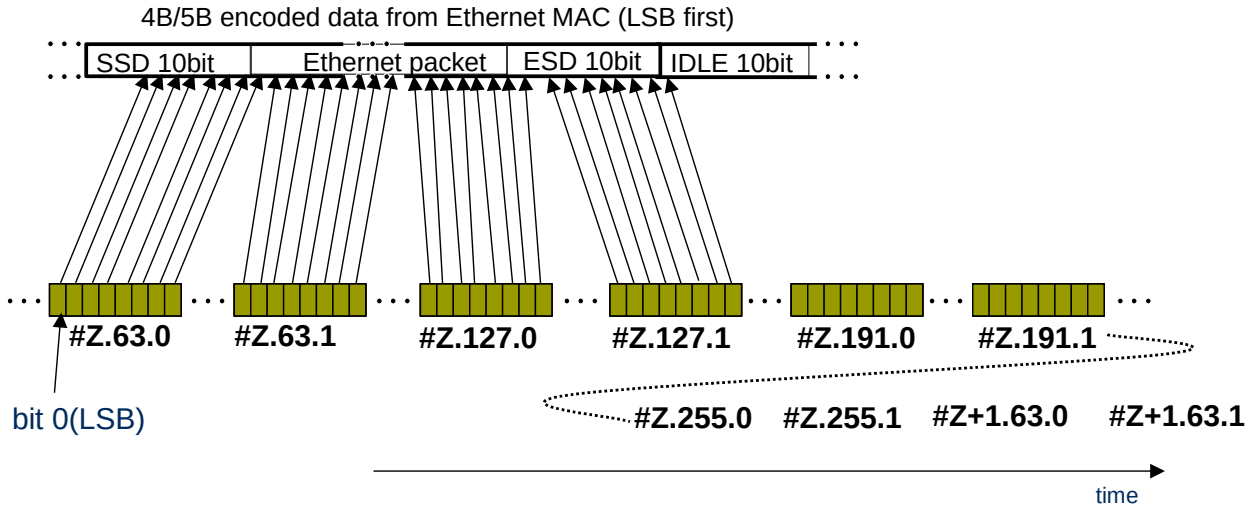


Figure 23: Example showing the mapping of control BYTES to Ethernet channel at 1228.8Mbit/s CPRI line bit rate and pointer BYTE #Z.194.0=rr111111

4.2.7.7.3. Minimum C&M Channel Support

The use of either HDLC or Ethernet is optional. It is recommended for each REC or RE to support at least one non-zero C&M channel bit rate on at least one link.

4.2.7.7.4. Passive Link

A passive link does not support any C&M channel. It may be requested by the master port indicating #Z.66.0 = rrrr r000 and #Z.194.0 = rr00 0000 (r = reserved, transmit 0, receiver don't care) in downlink.

4.2.7.8. Future Protocol Extensions

There are 36 control words of one hyperframe reserved for future interface protocol extensions. Reserved words are completely filled with reserved bits (reserved bits are marked with "r"). This means that a transmitter shall send 0's for bits marked with "r", and the receiver shall not interpret bits marked with "r". (transmit: r = 0, receiver: r = don't care).

4.2.7.9. Vendor Specific Data

Depending on the usage of the fast C&M channel up to 192 control words (in subchannels 16 to 63) of one hyperframe are available for vendor specific data. A minimum of 16 control words (in subchannels 16 to 19) per hyperframe are reserved for vendor specific data.

4.2.7.10. Control AxC Data

Up to 16 control words (in subchannels 4 to 7) of one hyperframe are available for AxC specific control data. In each hyperframe AxC specific Control Data streams (Ctrl_AxC) with dedicated numbers Ctrl_AxC# are allocated with a granularity of two bytes according to the following rule:

Low byte: Ctrl_AxC# = Y*8 + Xs + (Ns - 4)*4, with Ns $\in$ {4, 5}

High byte: Ctrl_AxC# = Y*8 + Xs + (Ns - 6)*4, with Ns $\in$ {6, 7}

with

Y = 0,…,T_{CW}/8-1

Xs = 0,…,3

The resulting allocation scheme is shown in Figure 23Z. T_{CW} x 2 bytes are reserved per hyperframe with Parameter T_{CW} defined in Table 3.

The mapping of Ctrl_AxC with number Ctrl_AxC# to AxCs is not defined in CPRI but is vendor specific. The same applies for the actual content of the control data bytes.

The given Control AxC Data scheme is one possibility to transmit associated AxC specific control data in GSM (e.g. GSM frequency hopping information), but may be also used for other purposes, e.g. real time RTWP measurement reporting in UMTS.

		Xs 0	1	2	3	
Ns=4	Y=0	Ctrl_AxC#0	Ctrl_AxC#1	Ctrl_AxC#2	Ctrl_AxC#3	low byte area
	Y=1	Ctrl_AxC#8	Ctrl_AxC#9	Ctrl_AxC#10	Ctrl_AxC#11	
	...	...	...	...	...	
	Y=T_{CW}/8-1	Ctrl_AxC#(T_{CW}-8)	Ctrl_AxC#(T_{CW}-7)	Ctrl_AxC#(T_{CW}-6)	Ctrl_AxC#(T_{CW}-5)	
Ns=5	Y=0	Ctrl_AxC#4	Ctrl_AxC#5	Ctrl_AxC#6	Ctrl_AxC#7	
	Y=1	Ctrl_AxC#12	Ctrl_AxC#13	Ctrl_AxC#14	Ctrl_AxC#15	
	...	...	...	...	...	
	Y=T_{CW}/8-1	Ctrl_AxC#(T_{CW}-4)	Ctrl_AxC#(T_{CW}-3)	Ctrl_AxC#(T_{CW}-2)	Ctrl_AxC#(T_{CW}-1)	
Ns=6	Y=0	Ctrl_AxC#0	Ctrl_AxC#1	Ctrl_AxC#2	Ctrl_AxC#3	high byte area
	Y=1	Ctrl_AxC#8	Ctrl_AxC#9	Ctrl_AxC#10	Ctrl_AxC#11	
	...	...	...	...	...	
	Y=T_{CW}/8-1	Ctrl_AxC#(T_{CW}-8)	Ctrl_AxC#(T_{CW}-7)	Ctrl_AxC#(T_{CW}-6)	Ctrl_AxC#(T_{CW}-5)	
Ns=7	Y=0	Ctrl_AxC#4	Ctrl_AxC#5	Ctrl_AxC#6	Ctrl_AxC#7	
	Y=1	Ctrl_AxC#12	Ctrl_AxC#13	Ctrl_AxC#14	Ctrl_AxC#15	
	...	...	...	...	...	
	Y=T_{CW}/8-1	Ctrl_AxC#(T_{CW}-4)	Ctrl_AxC#(T_{CW}-3)	Ctrl_AxC#(T_{CW}-2)	Ctrl_AxC#(T_{CW}-1)	

Figure 23Z: Control AxC Data allocation scheme

4.2.8. Synchronization and Timing

The RE shall use the incoming bit clock at the slave port where the SAP_S is assigned as the source for the radio transmission and any link transmission bit clock. The time information is transferred from the REC to the RE through the information described in Section 4.2.7.5. The CPRI 10ms frame delimitation is provided by the Sync Byte (Z.0.0) of the hyperframe number #0.

4.2.8.1. UMTS frame timing

The UMTS radio frame is identical to the CPRI 10ms frame.

In this document the term "UMTS radio frame" is used for the UTRA FDD 10ms frame as well as for the E-UTRA 10ms frame.

4.2.8.2. WiMAX frame timing

The WiMAX frame timing is defined relative to CPRI 10ms frame timing per AxC or **AxC Group**. Uplink and downlink may have different WiMAX frame timing[6].

The WiMAX frame per **AxC Group** in a CPRI link is typically aligned with CPRI 10ms frame, especially in the non-networking case, but may not be aligned with the CPRI 10ms frame and may not be aligned with the WiMAX frame of other **AxC Groups** in general, especially in the networking case. The REC informs the RE about the timing offset between the CPRI frame and the WiMAX frame per **AxC Group** via the C&M plane channel. The offset is defined as follows and shown in the Fig. 23A. As the length of a WiMAX frame is an integer multiple of the CPRI basic frame (e.g. 5ms = 19200 CPRI basic frames), the frame boundary of each WiMAX frame is identified by this offset and WiMAX frame length in CPRI basic frames.

WiMAX Frame Offset:

The timing difference between the first CPRI basic frame (the basic frame number #0, the hyperframe number #0 and the BFN number #0) and the first basic frame of the WiMAX Frame assigned to the **AxC Group**.

[6] This WiMAX frame timing is not the actual WiMAX frame timing of the air interface but is the reference timing between REC and RE in WiMAX timing domain. This is similar to BFN in UMTS which is not identical to SFN or CFN.

The first basic frame of the WiMAX Frame is always aligned with the first basic frame of an **AxC Container Block**. The WiMAX frame duration is an integer multiple of the **AxC Container Block** duration.

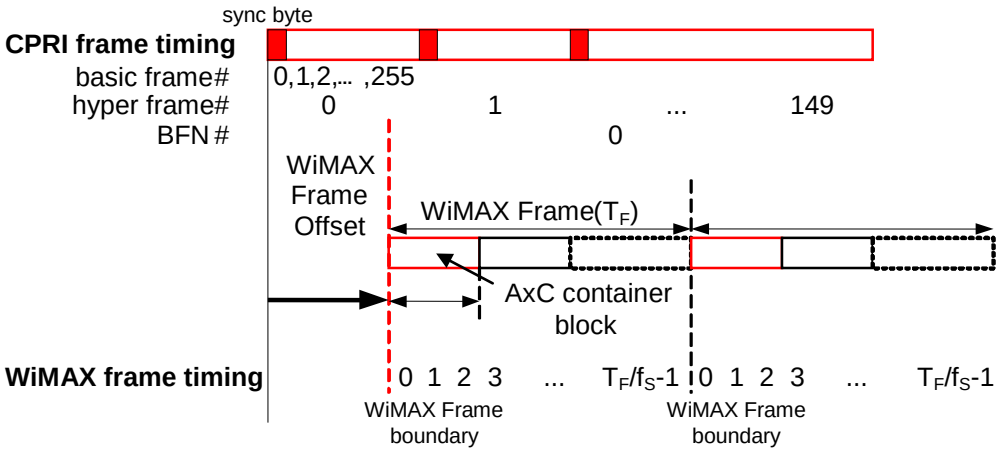


Figure 23A: WiMAX frame offset within CPRI frame timing

4.2.8.3. GSM frame timing

The GSM frame timing is defined relative to CPRI 10ms frame timing and BFN per AxC or **AxC Group**. The REC shall inform the RE about the timing relation between GSM frame and CPRI 10ms frame via the C&M plane channel.

- Uplink and downlink may have different GSM frame timing.
- As the GSM frame length is 60/13ms, every “13 x GSM frame” is mapped on “6 x CPRI frame” (60ms).
- The first GSM frame of every “13 x GSM frame” in a CPRI link is typically aligned with CPRI 10ms frame, especially in the non-networking case. However, in the networking case it will generally be the case that the start of the “13 x GSM frame” and CPRI 10ms frame are not aligned.
- The first CPRI basic frame of the first GSM frame of every “13 x GSM frame” is always aligned with the first CPRI basic frame of an **AxC Container Block**.
- The timing relation between GSM frames and CPRI 10ms frame is shown in Figure 23B. The BFN value m used as timing reference is only valid during one specific BFN cycle (4096 CPRI 10ms frames) since the BFN cycle is not an integer multiple of 60ms.

GSM Frame Offset:

The timing difference between the first CPRI basic frame of the m-th CPRI 10ms frame and the first CPRI basic frame assigned to the n-th GSM frame. “n” is selected so that the first CPRI basic frame of the n-th GSM frame is aligned with the first CPRI basic frame of an **AxC Container Block**. “m” is selected so that the “GSM Frame offset” is greater than or equal to “0” and less than “38400 CPRI basic frames”.

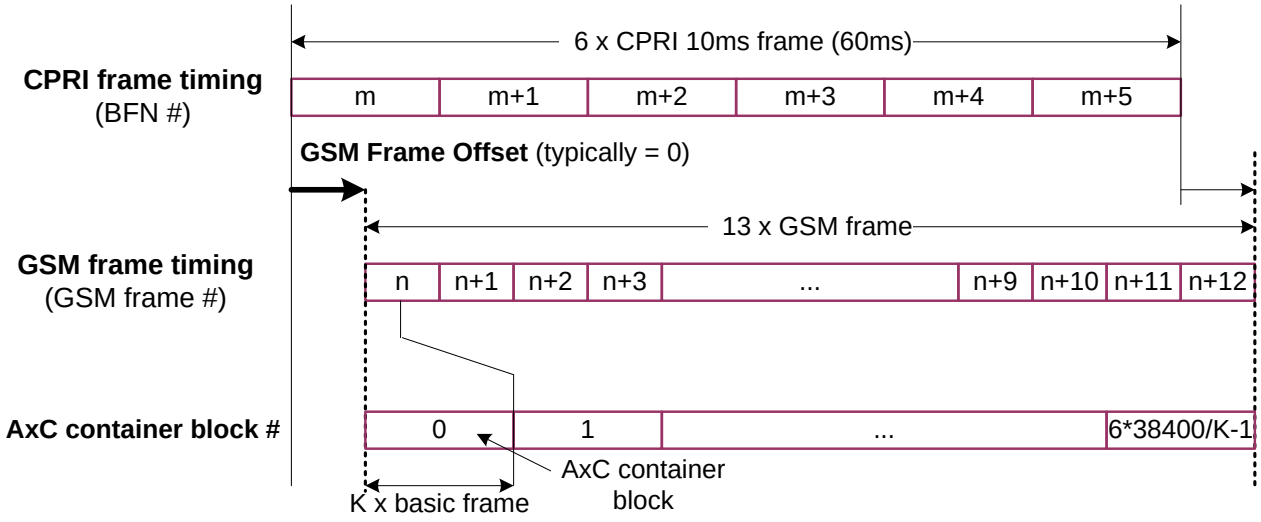


Figure 23B: The timing relation between GSM frames and CPRI 10ms frames

4.2.9. Link Delay Accuracy and Cable Delay Calibration[7]

The interface provides the basic mechanism to enable calibrating the cable delay on links and the round trip delay on multi-hop connections. More specifically, the reference points for delay calibration and the timing relation between input and output signals at RE are defined. All definitions and requirements in this section are described for a link between REC and RE. However, it shall also apply for links between two REs if the master port of the REC is replaced by a master port of a RE.

4.2.9.1. Definition of Reference Points for Cable Delay Calibration

The reference points for cable delay calibration are the input and the output points of the equipment, i.e. the connectors of REC and RE as shown in Figure 24 and Figure 24A. Figure 24 shows the single-hop configuration and Figure 24A shows the multi-hop configuration.

Reference points R1-4 correspond to the output point (R1) and the input point (R4) of REC, and the input point (R2), and the output point (R3) of an RE terminating a particular logical connection between SAP_{IQ}. The antenna is shown as “Ra” for reference.

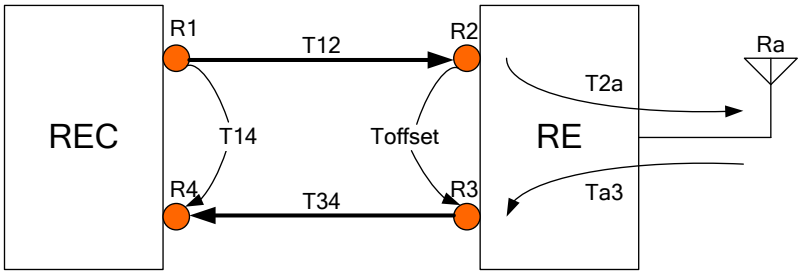


Figure 24: Definition of reference points for delay calibration (single-hop configuration)

Reference points RB1-4 in the networking RE correspond to the input point (RB2) and the output point (RB3) of the slave port and the output point (RB1) and the input point (RB4) of the master port.

[7] This section describes the single-hop configuration and the multi-hop configurations with networking RE(s) only. This section may be applied to any other multi-hop configurations including networking REC(s). See section 6.3.8 for further explanation.

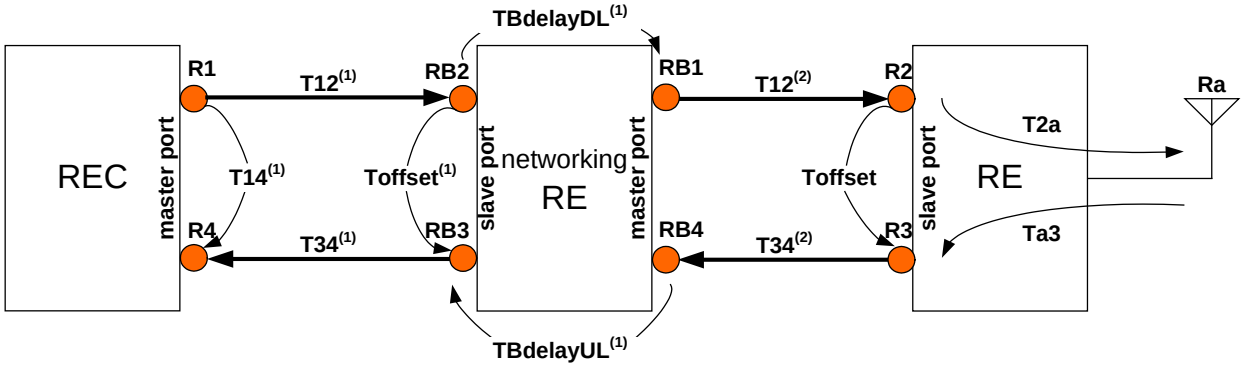


Figure 24A: Definition of reference points for delay calibration (multi-hop configuration)

4.2.9.2. Relation between Downlink and Uplink Frame Timing

Any RE shall use the incoming frame timing at the slave port where SAP_S is assigned as synchronization source (RB2 and R2, respectively) as the timing reference for any outgoing signals. The timing specifications are defined as follows. The single-hop case is explained first using Figure 25, then the multi-hop case is explained using Figure 25A.

Figure 25 shows the relation between downlink and uplink frame timing for the single-hop configuration.

- **T12** is the delay of downlink signal from the output point of REC (**R1**) to the input point of RE (**R2**).
- **T34** is the delay of uplink signal from the output point of RE (**R3**) to the input point of REC (**R4**).
- **Toffset** is the frame offset between the input signal at **R2** and the output signal at **R3**.
- **T14** is the frame timing difference between the output signal at **R1** and the input signal at **R4**.

RE shall determine the frame timing of its output signal (uplink) to be the fixed offset (**Toffset**) relative to the frame timing of its input signal (downlink). This fixed offset (**Toffset**) is an arbitrary value, which shall be greater than or equal to 0 and less than 256 T_C. In case the system shall fulfil R-21 and R-21A (delay calibration) then Toffset accuracy shall be better than ±8.138ns (=T_C/32). Different REs may use different values for **Toffset**. REC shall know the value of **Toffset** of each RE in advance (e.g. pre-defined value or RE informs REC by higher layer message). In addition, the downlink BFN and HFN from REC to RE shall be given back in uplink from the RE to the REC. In case of an uplink signalled LOS, LOF, RAI or SDI the REC shall treat the uplink BFN and HFN as invalid.

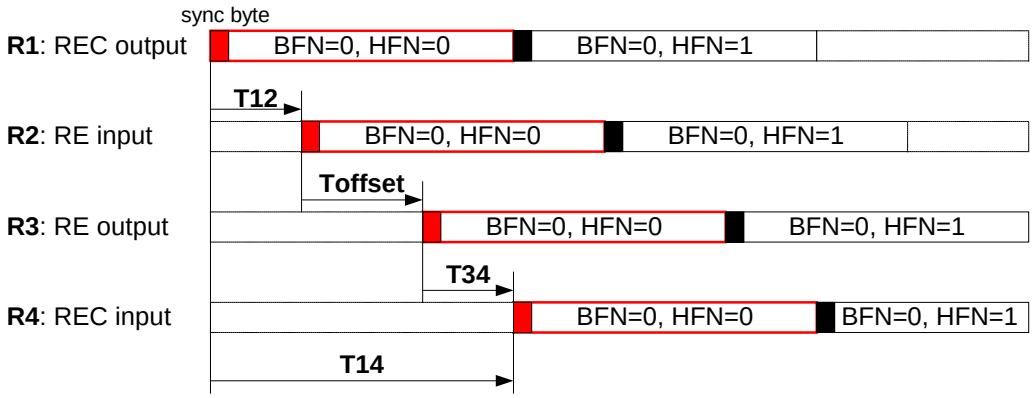


Figure 25: Relation between downlink and uplink frame timing (single-hop configuration)

Figure 25A shows the relation between downlink and uplink frame timing for multi-hop configuration.

The end-to-end delay definitions (**T12**, **T34** and **T14**) and the frame timing offset (**Toffset**) for a multi-hop connection are the same as those of the single-hop configuration.

The delay of each hop, the frame timing offset and the internal delay in each networking RE are defined as follows:

M is the number of hops for the multi-hop connection, where **M**>=2.

T12$^{(i)}$, **T34**$^{(i)}$ and **T14**$^{(i)}$ (1<=i<=**M**) is the delay of downlink signal, the delay of uplink signal and the frame timing difference between downlink and uplink of i-th hop respectively.

Toffset$^{(i)}$ (1<=i<=**M**) is the frame offset between the input signal at **RB2** and the output signal at **RB3** of the i-th RE. **Toffset**$^{(M)}$ = **Toffset**.

TBdelayDL$^{(i)}$ (1<=i<=**M**-1) is the delay of downlink signal between **RB2** and **RB1** of the i-th networking RE.

TBdelayUL$^{(i)}$ (1<=i<=**M**-1) is the delay of uplink signal between **RB4** and **RB3** of the i-th networking RE.

The timing specifications are as follows:

The same rule is applied for **Toffset**$^{(i)}$ (1<=i<= **M**) as for **Toffset** of a single-hop configuration.

Each networking RE shall determine the frame timing of its output signal (downlink) at **RB1** to be the fixed delay (**TBdelayDL**$^{(i)}$) relative to the frame timing of its input signal (downlink) at **RB2**. The frame position of downlink **AxC Container** (BFN, HFN and basic frame number) shall be kept unchanged. The position of **AxC Container** in a basic frame may be changed.

Each networking RE may change the frame position (BFN, HFN and basic frame number) of uplink **AxC Container** carrying a particular IQ sample(s) to minimize the delay between **RB4** and **RB3**. (This is applicable only when the contents in **AxC Containers** are not modified, i.e. the bit position of a particular IQ sample in **AxC Container** is kept unchanged). The difference of the frame position at RB3 relative to RB4 transferring the same uplink **AxC Container** shall be reported to the REC. The unit of the difference of frame positions is “basic frame”. In Figure 25A, the **AxC Container** in the frame position (BFN=0, HFN=0 and basic frame number=0) at RB4 is transferred in the frame position (BFN=0, HFN=0 and basic frame number=**N**$^{(i)}$). In this case the networking RE shall report the value “**N**$^{(i)}$” to the REC as the difference of frame positions of uplink **AxC Container**.

The end-to-end frame timing difference **T14** has the following relation with the 1st hop frame timing difference **T14**$^{(1)}$:

T14= **T14**$^{(1)}$ + **N** x T_C, where T_C is the basic frame length and **N** is calculated as $N = \sum_{i=1}^{M-1} N^{(i)}$.

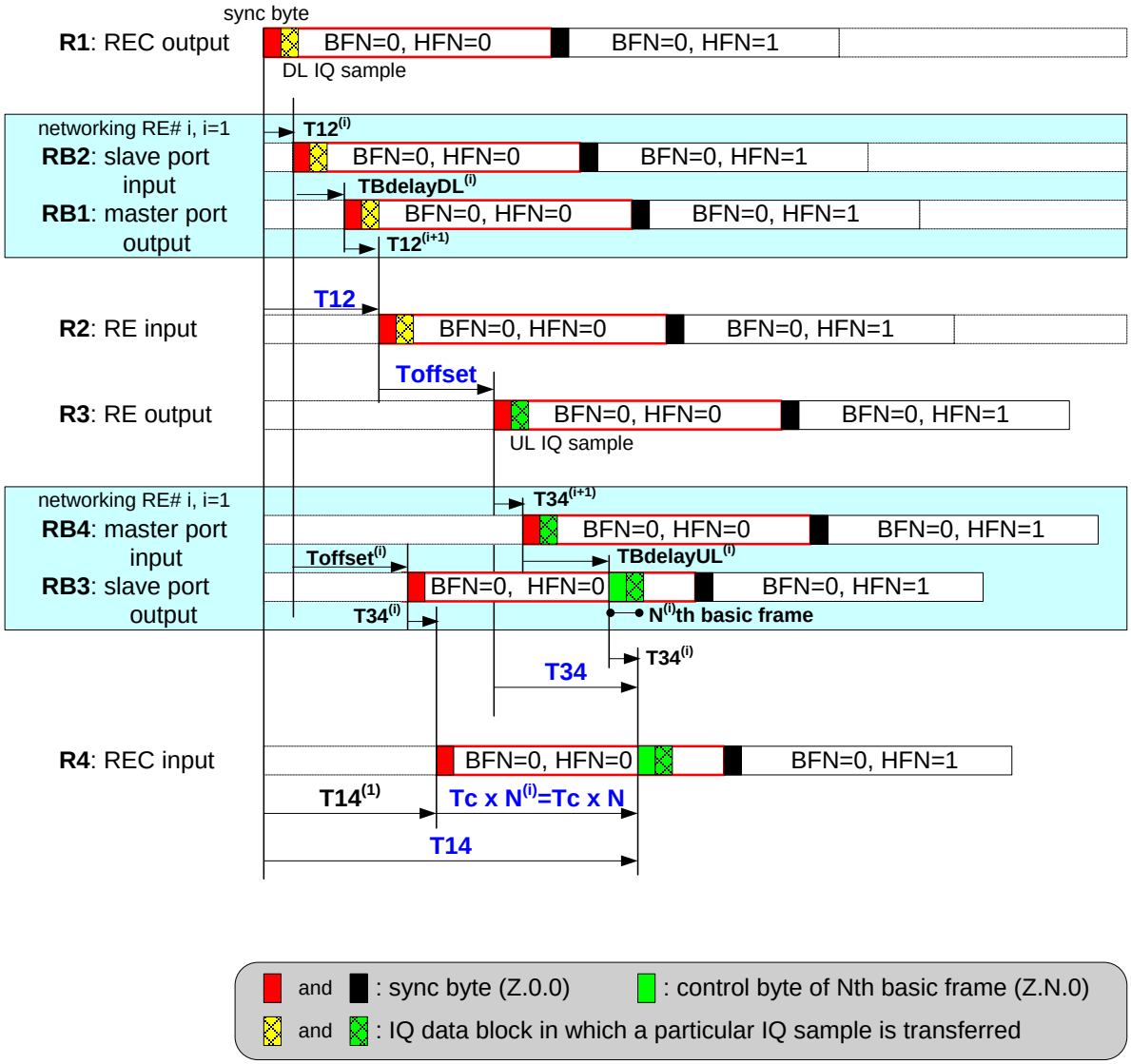


Figure 25A: Relation between downlink and uplink frame timing (multi-hop configuration)

4.2.9.3. Definition of Reference Points for Link Delay Accuracy

The reference points for the link delay accuracy and the round trip delay accuracy according to baseline requirements R-19 and R-20, respectively, are the service access points SAP_S. The cable delays with their reference points, as defined in section 4.2.9.1, are excluded from the link delay accuracy requirements. In case the system shall fulfil R-19 (link delay accuracy) then the accuracy of $TBdelayUL^{(i)}$ and $TBdelayDL^{(i)}$ which the REC is informed about shall be better than ±8.138ns ($=T_C/32$).

4.2.10. Link Maintenance of Physical Layer

4.2.10.1. Definition

Four layer 1 alarms are defined

- Loss of Signal (LOS)

- Loss of Frame (LOF)
- Remote Alarm Indication (RAI)
- SAP Defect Indication (SDI)

For each of these alarms a bit is allocated in the CPRI hyperframe to remotely inform the far-end equipment of the occurrence of the alarm.

On detection of the alarm at near end the inband bit is immediately (depending on the performance of the module) set and forwarded on CPRI to the far end. When the alarm is cleared the inband bit is reset.

Notice that to be able to receive and decode such information, the remote equipment must be at least in state C of start-up (for state definition, see Section 4.5).

Local actions are undertaken at both near and far end when failure is detected.

Failure is:

- defined when the alarm persists.
- set after time filtering of the alarm.
- cleared after time filtering of the alarm.

The timers for near and far end filtering are defined by the application layer.

4.2.10.2. Loss of Signal (LOS)

4.2.10.2.1. Detection

For 8B/10B line coding:

The CPRI definition of LOS is when at least 16 8B/10B violations occur among a whole hyperframe.

For 64B/66B line coding:

1st option for LOS:

The CPRI definition of LOS is when at least 4 64B/66B sync header code violations occur among a whole hyperframe.

2nd option for LOS:

The CPRI definition of LOS is when the 10GBASE-R PCS hi_ber variable (as defined in clause 49.2.13.2.2 of [22]) is set to “true”.

For optical mode of CPRI, detection of LOS may also be achieved by detecting light power below a dedicated threshold. Detection speed shall be within one hyperframe duration.

4.2.10.2.2. Cease

For 8B/10B line coding:

The alarm is cleared when a whole hyperframe is received without code violation.

For 64B/66B line coding:

1st option for LOS:

The alarm is cleared when a whole hyperframe is received without sync header code violation.

2nd option for LOS:

The alarm is cleared when the 10GBASE-R PCS hi_ber variable (as defined in clause 49.2.13.2.2 of [22]) is set to “false”.

4.2.10.2.3. Inband Bit

The inband bit that transport this information is #Z.130.0 b3

4.2.10.2.4. Local Action

RE

Upon detecting such a failure, the RE shall go into state B of the start-up sequence (see Section 4.5). In addition it is HIGHLY recommended that appropriate actions be performed to prevent from emitting on the radio interface.

REC

On detecting such a failure, the REC shall go into state B of the start-up sequence.

4.2.10.2.5. Remote Action

RE

When detecting such a failure, based on the received information, the RE shall go into state B of the start-up sequence.

In addition it is HIGHLY recommended that appropriate actions be performed to prevent from emitting on the radio interface.

REC

When detecting such a failure, based on the received information, the REC shall go into state B of start-up sequence.

4.2.10.3. Loss of Frame (LOF)

4.2.10.3.1. Detection

This alarm is detected if the hyperframe alignment cannot be achieved or is lost as shown in Figure 26.

Number of XACQ state and XSYNC state is restricted to acquisition time limitation. Figure 26 shows 2 XACQ and 3 SYNC states as an example.

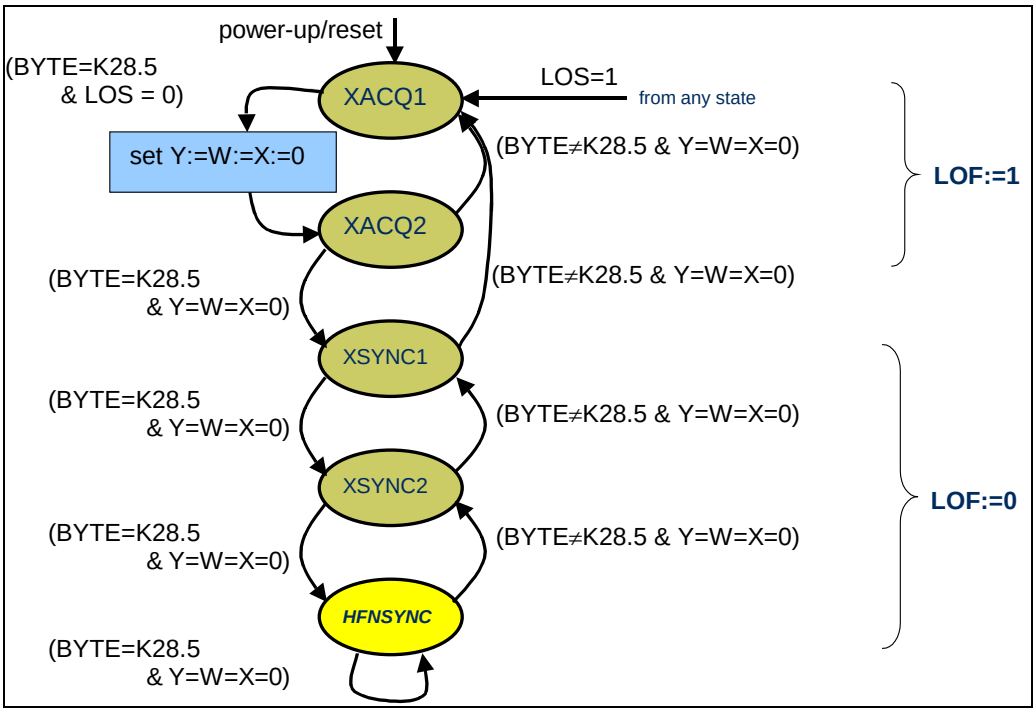


Figure 26: Example for LOF and HFNSYNC detection (8B/10B line coding)

For 8B/10B line coding option, receivers with highest available protocol version 2, figure 26A applies instead of figure 26. However, it may use figure 26 if it receives protocol version 1 from the transmitter. For 64B/66B line coding option figure 26B applies.

In the example given in figure 26A 32 bits are used for checking the descrambling sequence.

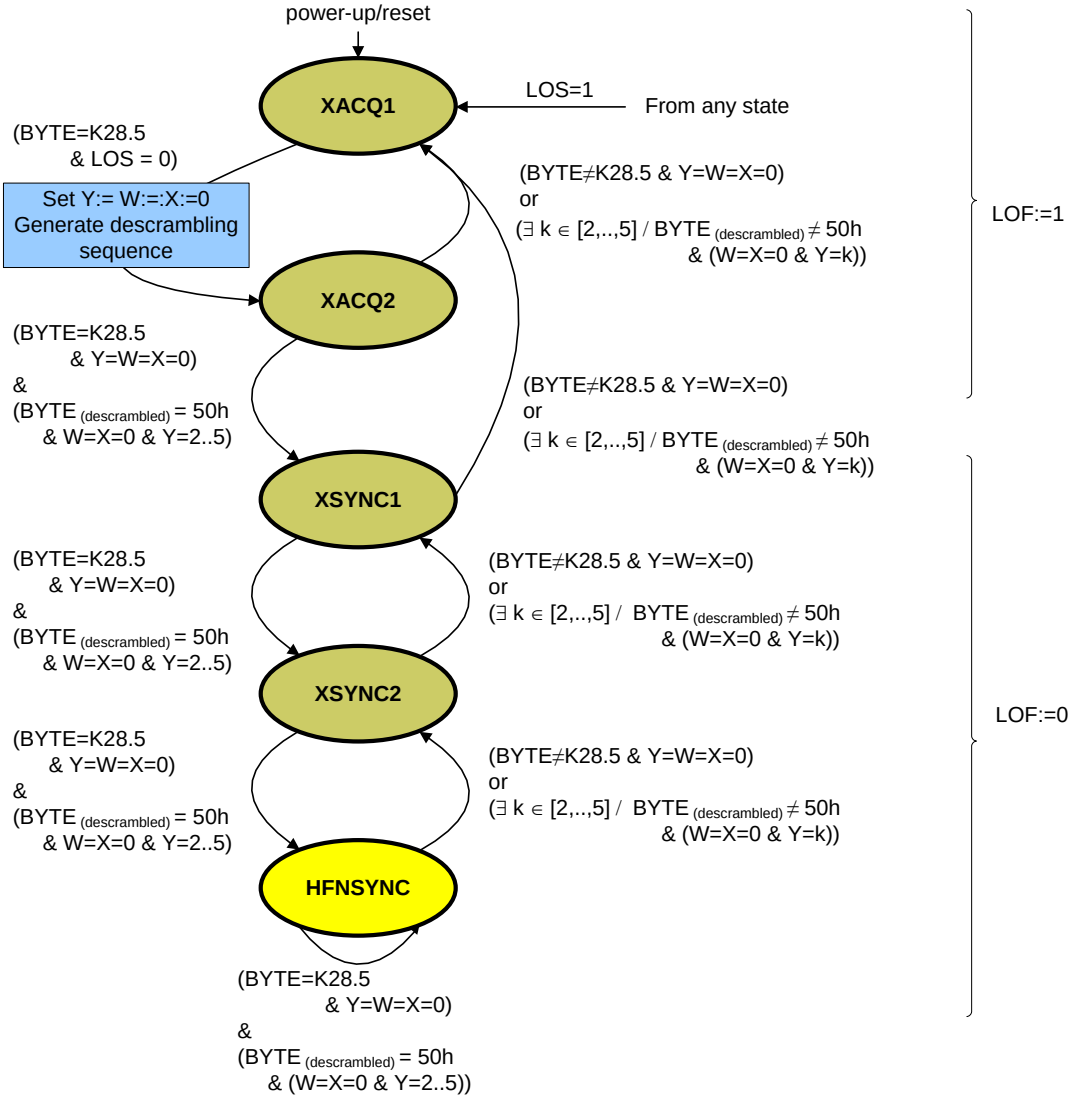


Figure 26A: Example for LOF and HFNSYNC detection (8B/10B line coding)

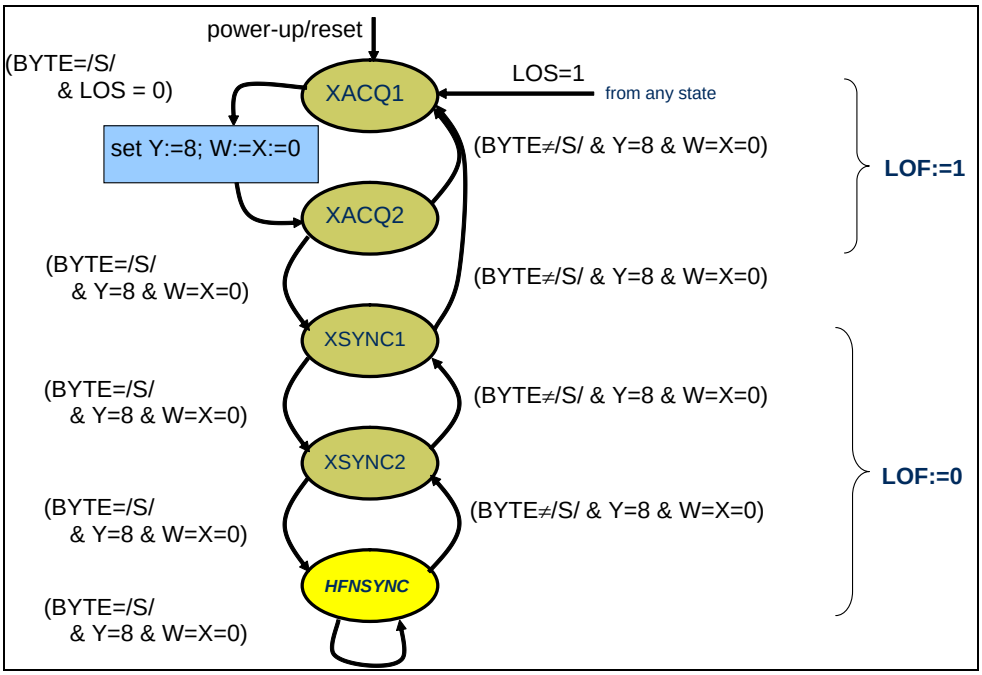


Figure 26B: Example for LOF and HFNSYNC detection (64B/66B line coding)

4.2.10.3.2. Cease

This alarm is cleared if the hyperframe alignment is achieved as shown in Figure 26, Figure 26A and Figure 26B.

4.2.10.3.3. Inband Bit

The inband bit that transports this information is #Z.130.0 b4

4.2.10.3.4. Local Action

RE

When detecting such a failure the RE shall go in state B of start-up sequence.

In addition it is HIGHLY recommended that appropriate actions be performed to prevent emission on the radio interface.

REC

When detecting such a failure, based on the received information, the REC shall go in state B of start-up sequence.

4.2.10.3.5. Remote Action

RE

When detecting such a failure, based on the received information, the RE shall go in state B of start-up sequence.

In addition it is HIGHLY recommended that appropriate actions be performed to prevent emission on the radio interface.

REC

When detecting such a failure, based on the received information, the REC shall go in state B of start-up sequence.

4.2.10.4. Remote Alarm Indication

4.2.10.4.1. Detection

Any errors, including LOS and LOF, that are linked to CPRI transceiver are indicated by the RAI information.

4.2.10.4.2. Cease

When no errors, including LOS and LOF, are linked to the CPRI transceiver, the RAI is cleared.

4.2.10.4.3. Inband Bit

The Remote Alarm Indication bit is used to transport this information: #Z.130.0 b1

4.2.10.4.4. Local Action

RE

Out of scope of CPRI.

REC

Out of scope of CPRI.

4.2.10.4.5. Remote Action

RE

When detecting such a failure, based on the received information, the RE shall go in state B of start-up sequence.

In addition it is HIGHLY recommended that appropriate actions be performed to prevent from emitting on the radio interface.

REC

When detecting such a failure, based on the received information, the REC shall go in state B of start-up sequence.

4.2.10.5. SAP Defect Indication

A link is said to be in “alarm” when the near end explicitly informs the far end equipment that the link shall not be used for any of the Service Access Points.

Notice in this case the CPRI link is fully available and decoded by the far end receiver.

4.2.10.5.1. Detection

The detection procedure is outside the scope of CPRI. This is fully application dependant.

4.2.10.5.2. Cease

The alarm reset procedure is outside the scope of CPRI. This is fully application dependant.

4.2.10.5.3. Inband Bit

The SAP Defect Indication Signal bit is used to transport this information: #Z.130.0 b2

4.2.10.5.4. Local Action

RE

N/A

REC

N/A

4.2.10.5.5. Remote Action

RE

The RE shall not use this link anymore for any of the CPRI Service Access Points: IQ, Sync or C&M. In addition it is HIGHLY recommended that appropriate actions be performed to prevent from emitting on the radio interface.

REC

The REC shall not use this link anymore for any of the CPRI Service Access Points: IQ, Sync or C&M.

4.2.10.6. Link quality monitoring

For 64B/66B line coding:

The number of sync header violations shall be counted and presented to the higher layers. The management of this information by higher layers is out of the scope of CPRI.

For 8B/10B line coding:

The link quality monitoring is optional.

In case link quality monitoring is supported the number of code violations shall be counted and presented to the higher layers. The management of this information by higher layers is out of the scope of CPRI.

4.3. Data Link Layer (Layer 2) Specification for Slow C&M Channel

CPRI slow C&M Data Link Layer shall follow the HDLC standard ISO/IEC 13239:2002 (E) [10] using the bit oriented scheme.

4.3.1. Layer 2 Framing

HDLC data frames and layer 2 procedures shall follow [10]. In addition the CPRI layer 2 for the slow C&M channel shall fulfil the following additions:

- **Information Field Length**
  HDLC information field length in HDLC frames shall support any number of octets.
- **Bit Transmission Order of the Information Part**
  HDLC Information field bit transmission order in HDLC frames shall be least significant bit (LSB) first.
- **Address field**
  HDLC frames shall use a single octet address field and all 256 combinations shall be available. Extended address field shall not be used in HDLC data frames.
- **Frame Format**
  HDLC data frames shall follow the basic frame format according to ISO/IEC 13239:2002 (E) [10], chapter 4.1.1[8].

4.3.2. Media Access Control/Data Mapping

Media Access Control/Data Mapping shall follow chapter 4.2.7.7.1 of this specification.

4.3.3. Flow Control

CPRI slow C&M channel flow control shall follow HDLC standard ISO/IEC 13239:2002 (E) [10]. In addition CPRI layer 2 for the slow C&M channel shall fulfil the following additions:

[8] FCS transmission order in HDLC frames shall be most significant bit (MSB) first as defined in the HDLC standard.

- **Flags**
  HDLC frames shall always start and end with the flag sequence. A single flag must not be used as both the closing flag for one frame and the opening flag for the next frame.
- **Inter-frame time fill**
  'Inter-frame time fill' between HDLC frames shall be accomplished by contiguous flags.

4.3.4. Control Data Protection/ Retransmission Mechanism

CPRI slow C&M channel data protection shall follow HDLC standard ISO/IEC 13239:2002 (E) [10]. In addition CPRI layer 2 for the slow C&M channel shall fulfil the following addition:

- **Frame Check Sequence (FCS)**
  CPRI slow C&M channel shall support a FCS of length 16 bit as defined in ISO/IEC 13239:2002 (E) [10].

Retransmission mechanisms shall be accomplished by higher layer signalling.

4.4. Data Link Layer (Layer 2) Specification for Fast C&M Channel

CPRI C&M Fast Data Link Layer shall follow the Ethernet standard as specified in IEEE 802.3 [22].

4.4.1. Layer 2 Framing

Data mapping in layer 2 shall follow clause "3. Media access control frame structure" of IEEE 802.3 [22].

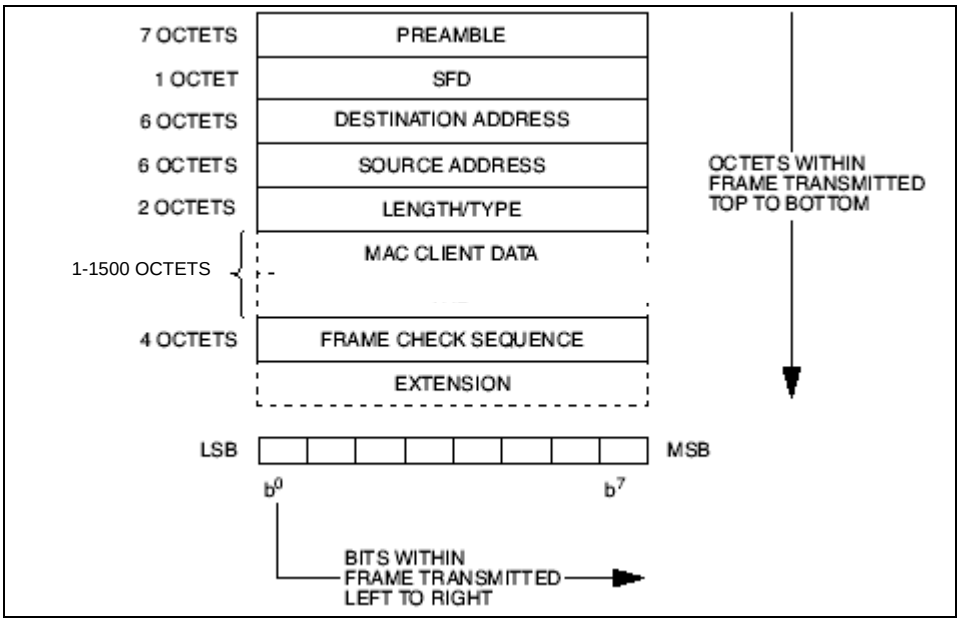


Figure 27: Layer 2 Framing

Specific CPRI requirements:

Minimum Ethernet frame length and padding:
Due to the specific CPRI framing, no minimum frame length makes any sense for CPRI application. CPRI does not specify any minimum frame size and does not require frame padding.

The MAC client Data + PAD field length shall range from 1 to 1500 octets.

Extension field:
The extension field shall not be used within CPRI.

4.4.2. Media Access Control/Data Mapping

Layer 2 data mapping in the CPRI frame is performed according to section "4.2.7.7.2 Fast C&M channel" of this specification.

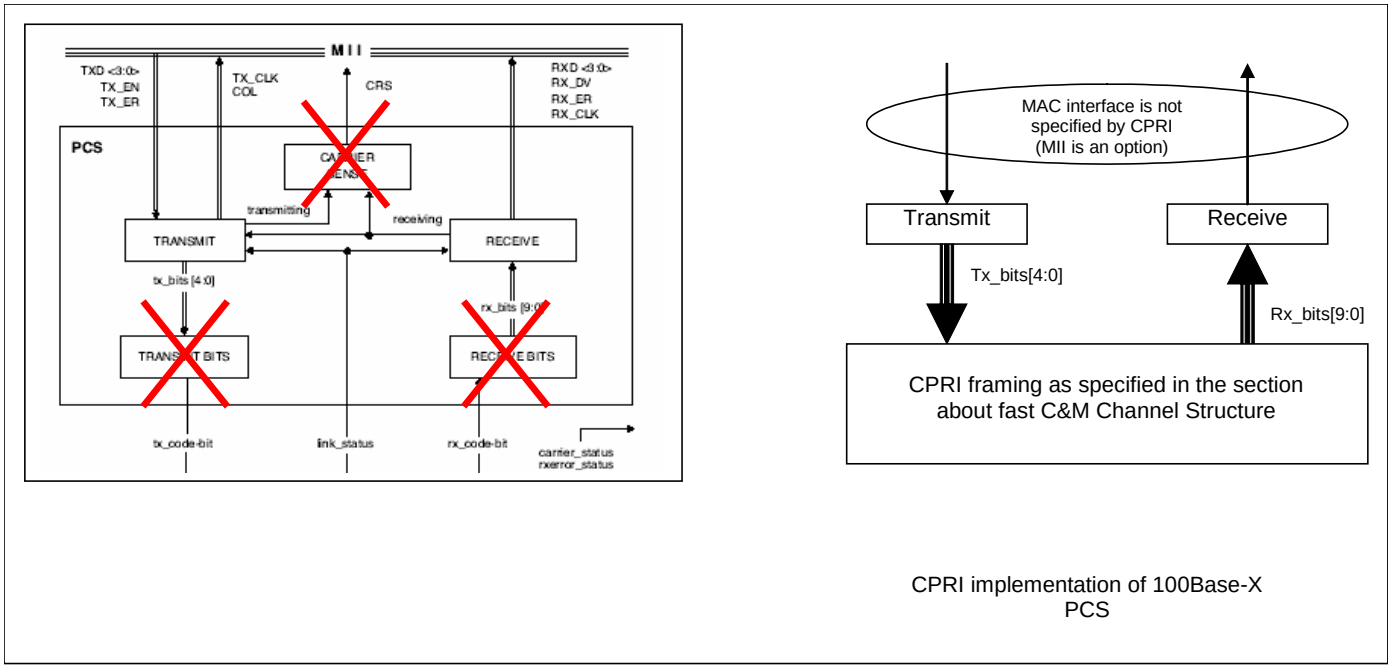
In addition the Ethernet frame shall be controlled and mapped through usage of clause “24.2 Physical Coding SubLayer (PCS)” of IEEE 802.3 [22] concerning 100BASE-X.

PCS supports 4 main features that are not all used by CPRI (see Table 13):

Table 13: PCS features used by CPRI

Feature	CPRI support
Encoding/Decoding	Fully supported by CPRI
Carrier sense detection and collision detection	*Irrelevant to CPRI*
Serialization/deserialization	*Irrelevant to CPRI*
Mapping of transmit, receive, carrier sense and collision detection	*Irrelevant to CPRI*

Figure 24-4 in “24. Physical Coding SubLayer (PCS) and Physical Medium Attachment (PMA) sublayer, type 100BASE-X” of IEEE 802.3 [22] is modified as shown in Figure 28:



CPRI implementation of 100Base-X PCS

Figure 28: CPRI implementation of 100BASE-X PCS

The Ethernet MAC frame shall be encoded using the 4B/5B code of 100BASE-X PCS (Physical Coding Sublayer) as specified in clause 24.2 of IEEE 802.3 [22].

The 4B/5B code list shall be according table 24.1 of IEEE 802.3 [22] (see below).

Table 14: 4B/5B code list (modified Table 24.1 of IEEE 802.3 [22])

	PCS code-group [4:0] 4 3 2 1 0	Name	MAC Client Data nibble	Interpretation
DATA	1 1 1 1 0	0	0 0 0 0	Data 0
	0 1 0 0 1	1	0 0 0 1	Data 1
	1 0 1 0 0	2	0 0 1 0	Data 2
	1 0 1 0 1	3	0 0 1 1	Data 3
	0 1 0 1 0	4	0 1 0 0	Data 4
	0 1 0 1 1	5	0 1 0 1	Data 5
	0 1 1 1 0	6	0 1 1 0	Data 6
	0 1 1 1 1	7	0 1 1 1	Data 7
	1 0 0 1 0	8	1 0 0 0	Data 8
	1 0 0 1 1	9	1 0 0 1	Data 9
	1 0 1 1 0	A	1 0 1 0	Data A
	1 0 1 1 1	B	1 0 1 1	Data B
	1 1 0 1 0	C	1 1 0 0	Data C
	1 1 0 1 1	D	1 1 0 1	Data D
	1 1 1 0 0	E	1 1 1 0	Data E
	1 1 1 0 1	F	1 1 1 1	Data F
	1 1 1 1 1	I	undefined	IDLE; used as inter-stream fill code
CONTROL	1 1 0 0 0	J	0 1 0 1	Start-of-Stream Delimiter, Part 1 of 2; always used in pairs with K
	1 0 0 0 1	K	0 1 0 1	Start-of-Stream Delimiter, Part 2 of 2; always used in pairs with J
	0 1 1 0 1	T	undefined	End-of-Stream Delimiter, Part 1 of 2; always used in pairs with R
	0 0 1 1 1	R	undefined	End-of-Stream Delimiter, Part 2 of 2; always used in pairs with T
INVALID	0 0 1 0 0	H	Undefined	Transmit Error; used to force signaling errors
	0 0 0 0 0	V	Undefined	Invalid code
	0 0 0 0 1	V	Undefined	Invalid code
	0 0 0 1 0	V	Undefined	Invalid code
	0 0 0 1 1	V	Undefined	Invalid code
	0 0 1 0 1	V	Undefined	Invalid code
	0 0 1 1 0	V	Undefined	Invalid code
	0 1 0 0 0	V	Undefined	Invalid code
	0 1 1 0 0	V	Undefined	Invalid code
	1 0 0 0 0	V	Undefined	Invalid code
	1 1 0 0 1	V	Undefined	Invalid code

The Ethernet frame shall be delineated by the PCS function as shown in Figure 29:

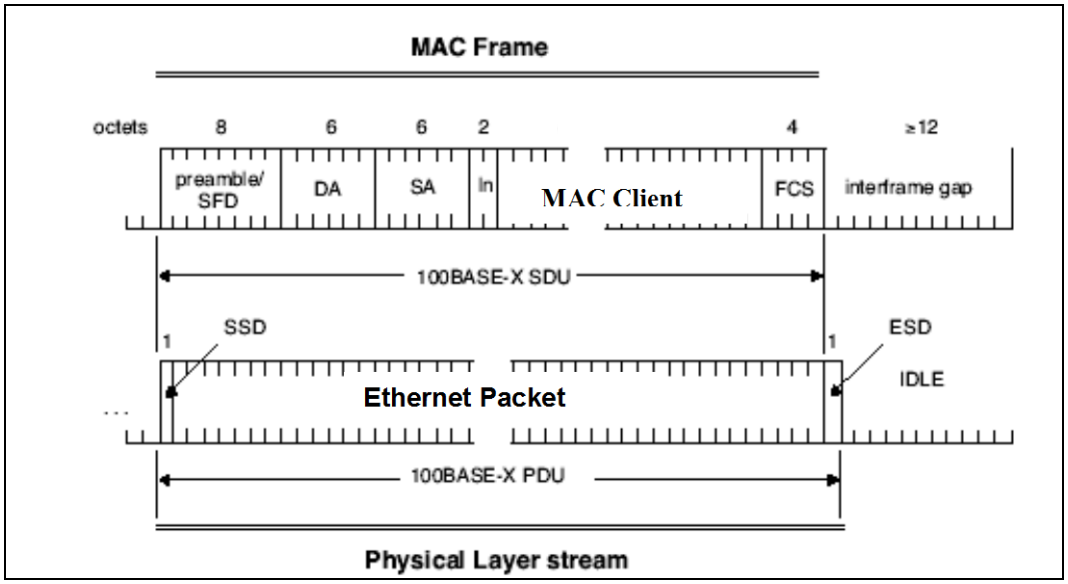


Figure 29: Physical Layer Stream of 100BASE-X

4.4.3. Flow Control

No flow control is provided for the fast C&M channel.

4.4.4. Control Data Protection/ Retransmission Mechanism

Data protection shall follow clause “3.2.9. Frame Check Sequence (FCS) field” of IEEE 802.3 [22]. No retransmission mechanism is specified for Fast C&M channel layer 2.

4.5. Start-up Sequence

This section defines the sequence of actions to be performed by master and slave ports connected by CPRI. When both the slave port and the master port are in state F or G, the link is in normal operation.

After a reset, any configurable ports of the RE shall be configured as slave ports. All ports of the RE shall enter state A. All the master ports of the RE shall remain in state A until at least one of the slave ports has been in state E.

4.5.1. General

The start-up procedure accomplishes two main things:

- Synchronization of layer 1: byte alignment and hyper frame alignment
- Alignment of capabilities of the master and slave ports: line bit rate, protocol, C&M channel bit rate, C&M protocol, vendor specific signalling

Since there is no mandatory line bit rate or C&M channel bit rate the master port and slave port shall, during the start-up procedure, try different configurations until a common match is detected. The common match does not have to be optimal – it shall be considered as just a first contact where capabilities can be exchanged for a proper configuration to be used in the following communication.

For all states, it is mandatory to always transmit information consistent with the protocol indicated in #Z.2.0 on all control words on subchannel 1 and subchannels 3 to 15.

When changing the line bit rate of the transmitted CPRI, the interruption of transmission shall be less than 0.1s. When changing the line bit rate of the received CPRI, the interruption of reception shall be less than 0.1s. The time to reach HFNSYNC for the receiving unit shall be less than 0.2s, given the precondition that the far-end transmitter is on, they use the same line bit rate and no bit errors occur.

In the negotiation steps in state C and D the master and slave ports shall sample and evaluate the received protocol version and C&M channel bit rates at a rate of at least every 0.1 s. The transmitted protocol version and C&M channel bit rates shall be updated within 0.2 s after the evaluation.

4.5.2. Layer 1 Start-up Timer

The start-up procedure may be endless due to two reasons:

- Fault in one of the units
- No common layer 1 protocol or C&M channel bit rate or C&M type.

The supervision may be done per state and per cause, but the start-up procedure also specifies a generic start-up timer which shall be set upon entry of the start-up procedure and shall be cleared when the C&M channel is established.

If the timer expires the start-up procedure shall be restarted.

The “layer 1 start-up timer” is activated in transitions 2, 5, 8, 12, 13, 15.

The “layer 1 start-up timer” is cleared in transitions 6, 9, 10, 11, 14 and in state E when the higher layer C&M connection is established.

If the “layer 1 start-up timer” expires, transition 16 shall take place and state B is entered, possibly modifying the available set of line bit rates and protocols.

The “layer 1 start-up timer” expiration time is vendor specific.

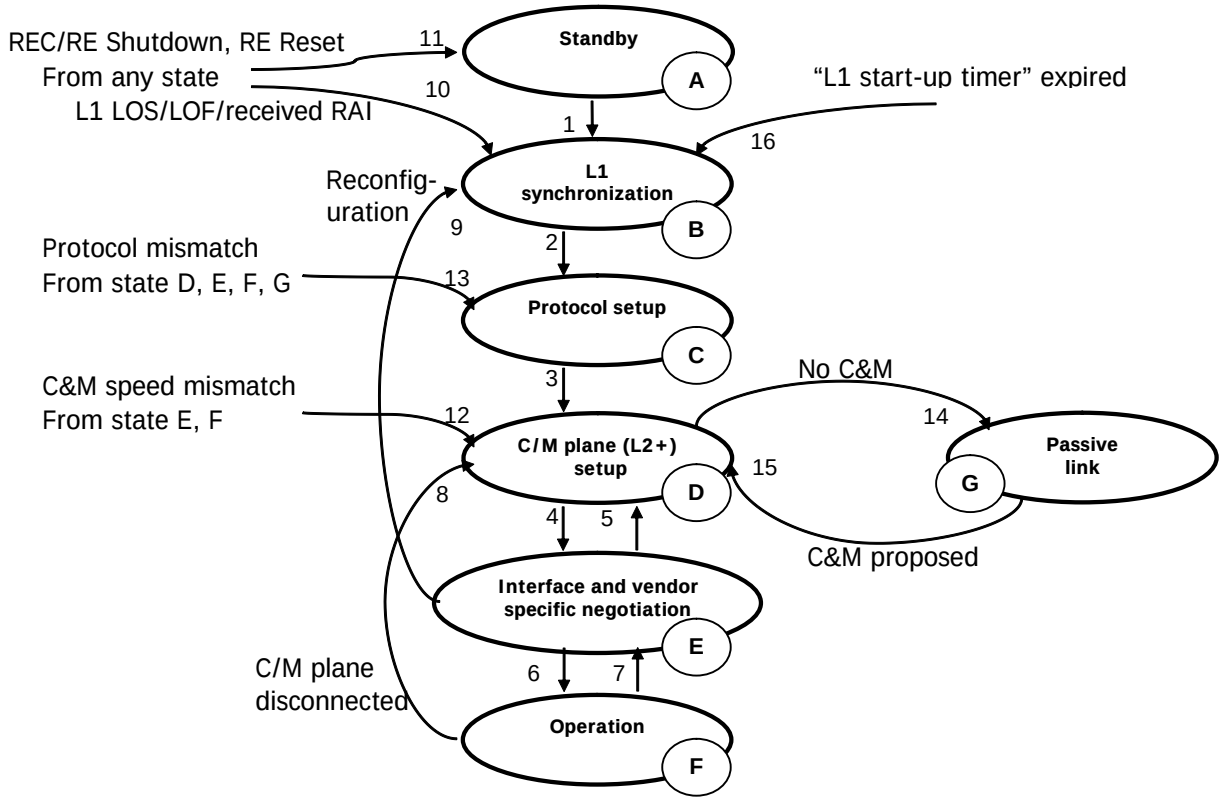


Figure 30: Start-up states and transitions

4.5.3. State Description

4.5.3.1. State A – Standby

Prerequisites:
None

Description:
Waiting to be configured to start up CPRI. No transmission or reception of CPRI. The operator may configure a suitable start-up configuration (line bit rate, C&M channel characteristics). The master and slave ports may also have knowledge about a previous successful configuration.

4.5.3.2. State B – L1 Synchronization and Rate Negotiation

Prerequisites:
The set of available line bit rate, protocol versions and C&M plane characteristics are known. This may be the complete set of the unit or a subset based on operator configuration or previous negotiation between the units (e.g. from state E).

Description:
During this state, the line bit rate of the interface is determined and both master and slave ports reach layer 1 synchronization up to state HFNSYNC.

Interpreted control BYTES:
For 8B/10B line coding protocol version 1 and 2; #Z.0.0, #Z.64.0
For 8B/10B line coding protocol version 2; #Z.0.2 … #Z.0.T/8-1 (see figure 26A)
For 64B/66B line coding; #Z.0.8, #Z.64.0

Master port actions:
The master port starts to transmit the CPRI at the highest available line bit rate directly when entering the state, and also start to attempt to receive a CPRI at the same line bit rate. If the master port does not reach synchronization state HFNSYNC it shall select another line bit rate from CPRI transmission after time T1 from entering the state, given that another line bit rate is available. T1 is 0.9-1.1 s. Each following T1 interval, a new line bit rate for reception and transmission shall be selected, given that another line bit rate is available. The line bit rates shall be selected from the available set in a round robin fashion, i.e. first highest, the second highest, …, the slowest, and then restarting from the highest line bit rate.

While in this state, the master port shall set the protocol version in #Z.2.0 to its highest available protocol version, and the C&M channel bit rates in #Z.66.0 and #Z.194.0 to its highest available C&M channel bit rates, for the transmitted line bit rate.

Slave port actions:
The slave port shall start attempting to receive CPRI at the highest available line bit rate directly when entering the state. If the slave port does not reach synchronization state HFNSYNC it shall select another line bit rate for CPRI reception after T1' from entering the state, given that another line bit rate is available. T1' is 3.9-4.1s. Each following T1' interval, a new reception line bit rate shall be selected for reception, given that another line bit rate is available. The line bit rates shall be selected from the available set in a round robin fashion, i.e. first highest, the second highest, …, the slowest, and then restarting from the highest line bit rate.

When entering this state, the slave port shall turn off its CPRI transmitter, if this state was entered with transition 10 the slave port may optionally transmit for a maximum of 5 hyperframes to indicate to far-end equipment the layer 1 link maintenance control BYTE #Z.130.0. When the slave port reaches synchronization state HFNSYNC, it shall start transmit CPRI on the same line bit rate.

While in this state, the slave port shall set the protocol version in #Z.2.0 according to the rule in state C, below, or to the highest available protocol version, for the transmitted bit rate. While in this state, the slave port shall set the C&M channel bit rates in #Z.66.0 and #Z.194.0 according to the rule in state D, or to the highest available C&M channel bit rate, for the transmitted line bit rate.

Comments:
While in this state, no timer to detect hanging-up is provided by the start-up procedure. Such a hanging-up will occur in case of HW fault or may also occur for configurations with a master port supporting more than 4

line bit rates for auto-negotiation. Such a hanging-up shall be detected and managed by vendor specific means. For more information see also annex 6.8.

4.5.3.3. State C – Protocol Setup

Prerequisites:
Layer 1 is synchronized, i.e., master-to slave and slave-to-master hyper frame structures are aligned.

Description:
During this state, a common protocol version of CPRI is determined.

Interpreted control BYTES:
For 8B/10B line coding; #Z.0.0, #Z.64.0, #Z.2.0
For 64B/66B line coding; #Z.0.8, #Z.64.0, #Z.2.0

Master port actions:
The master port shall select its highest available protocol version for the present line bit rate (see table 21) when entering this state. The protocol version shall be stated in #Z.2.0. When the master port receives a valid or an updated protocol version from the slave port,

- If the currently received protocol version is equal to the current protocol version sent by the master port, the protocol setup is achieved
- If the currently received protocol version differs from the current protocol version sent by the master port, it shall reselect the protocol version. The new protocol version shall be selected according to the rule:

  New master port protocol version = highest available protocol version which is less or equal to received slave port protocol version (received in #Z.2.0)

  Error case: If no such protocol exists:

  New master port protocol version = lowest available protocol version

Note that the reselection may choose the already transmitted protocol version. The new selected protocol version shall be stated in #Z.2.0. If the currently received protocol version is equal to the new protocol version sent by the master port, the protocol setup is achieved.

Slave port actions:
The slave port shall decode the received protocol version by looking at #Z.2.0 When the slave port receives a valid or an updated protocol version from the master port,

- If the currently received protocol version is equal to the current protocol version sent by the slave port, the protocol setup is achieved
- If the currently received protocol version differs from the current protocol version sent by the slave port, the slave port shall reselect the protocol version. The new proposed protocol version shall be selected according to the rule:

  New slave port protocol version = highest available protocol version which is less or equal to received master port protocol version (received in #Z.2.0)

  Error case: If no such protocol exists:

  New slave port protocol version = lowest available protocol version

Note that the reselection may choose the already transmitted protocol version. The new selected protocol version shall be stated in #Z.2.0. If the currently received protocol version is equal to the new protocol version sent by the slave port, the protocol setup is achieved.

Comments:
If the master port does not receive a new protocol version before the layer 1 start-up timer expires, it can assume that there are no common protocol versions. Such a detection can be made faster but then the application must take into account the case where the slave port enters the state after the master port. Layer 1 control bits can start to be interpreted but since they require error protection filtering (majority decision) the interpretation is not available until the subsequent state D.

4.5.3.4. State D – C&M Plane (L2+) Setup

Prerequisites:
Layer 1 is synchronized and the protocol is agreed on.

Description:
During this state, a common C&M channel bit rate is determined.

Interpreted control BYTES:
All

Master port actions:
The master port shall select its highest available C&M channel bit rate when entering this state: Highest available HDLC bit rate and highest available Ethernet bit rate. The bit rates shall be stated in #Z.66.0 and #Z.194.0. When the master port receives a valid or an updated bit rate in either #Z.66.0 or #Z.194.0 from the slave port,

- If at least one of the currently received bit rate is equal to the corresponding bit rate sent by the master port, the C&M plane setup is achieved
- If both currently received bit rates differ from the current bit rates sent by the master port, the master port shall reselect the C&M channel bit rate in #Z.66.0 and in #Z.194.0. Each new bit rate shall be selected according to the rule:

  New master port bit rate = highest available bit rate which is less or equal to received slave port bit rate (received in #Z.66.0 or #Z.194.0)

  Error case: The resulting bit rate according to the rule is “no link”, i.e. 0 bit rate:

  New master port bit rate = lowest available bit rate

Note that the reselection may choose the already transmitted C&M channel bit rates. The new selected bit rates shall be stated in #Z.66.0 and #Z.194.0. If at least one of the currently received bit rate is equal to the corresponding new bit rate sent by master port, the C&M plane setup is achieved.

In this state it is possible for the master port to send #Z.66.0 equal to “rrrr r111” if none of the pre-defined HDLC bit rates are suitable for a specific implementation. This requires that the node is aware in advance of the characteristics of the HDLC channel when transmitting value “rrrr r111” in #Z.66.0.

The master port shall check that #Z.2.0 is equal in both directions. If it is not equal it shall enter state C.

Slave port actions:
The slave port shall decode the received C&M channel bit rates by looking at both #Z.66.0 and #Z.194.0. When the slave port receives a valid or an updated bit rate in either #Z.66.0 or #Z.194.0 from the master port,

- If at least one of the currently received bit rates is equal to the corresponding bit rate sent by the slave port, the C&M plane setup is achieved
- If both currently received bit rates differ from the current bit rates sent by the slave port the slave port shall reselect the C&M channel bit rates for each C&M channel, i.e. on both #Z.66.0 and #Z.194.0. The new proposed C&M channel bit rates shall be selected according to the rule:

  New slave port bit rate = highest available bit rate which is less or equal to received master port bit rate (received in #Z.66.0 or #Z.194.0)

  Error case: The resulting bit rate according to the rule is “no link”, i.e. 0 bit rate:

  New slave port bit rate = lowest available bit rate

Note that the reselection may choose the already transmitted C&M channel bit rates. The new selected bit rates shall be stated in #Z.66.0 and #Z.194.0. If at least one of the currently received bit rates is equal to the corresponding new bit rate sent by the slave port, the C&M plane setup is achieved.

If the slave port received #Z.66.0 = "rrrr r111" from the master port and if the slave port node is aware in advance of the characteristics of the HDLC channel, it should send #Z.66.0 equal to "rrrr r111".

The slave port shall check that #Z.2.0 is equal in both directions. If it is not equal it shall enter state C.

Comments:
If the master port does not receive a new C&M channel bit rate proposal before the layer 1 start-up timer

expires, it can assume that there are no common C&M channel bit rates on this line bit rate. Such a detection can be made faster but then the application must take into account the case where the slave port enters the state after the master port. The negotiation results in a common C&M channel bit rate on at least one of the available C&M channels. While in this state, L1 inband protocol is interpreted which may lead to state G being entered.

4.5.3.5. State E – Interface and Vendor specific Negotiation

Prerequisites:
One C&M channel bit rate is agreed on.

Description:
During this state, application in master and slave ports negotiate the CPRI usage.

Interpreted control BYTES:
All

Master port actions:
If a common bit rate for the Ethernet link was agreed on in state D, it shall be used. Otherwise the HDLC link shall be used. In this state a negotiation to a HDLC bit rate that is not one of the pre-defined bit rates may take place. After the negotiation the master port will set #Z.66.0 to “rrrr r111” to indicate to the slave port that a new HDLC bit rate is used, the characteristic of the negotiated HDLC channel is vendor specific. The connection establishment and higher layer negotiation is outside the scope of the specification. When the connection is established the “layer 1 start-up timer” shall be cleared.

The master port shall check that #Z.2.0 is equal in both directions. If it is not equal it shall enter state C. The master port shall check that at least one of the values #Z.66.0 or #Z.194.0 is equal in both directions. If both differ, it shall enter state D.

Slave port actions:
If a common bit rate for the Ethernet link was agreed on in state D, it shall be used. Otherwise the HDLC link shall be used. In this state a negotiation to a HDLC bit rate that is not one of the pre-defined bit rates may take place. After the negotiation the slave port will set #Z.66.0 to “rrrr r111” to indicate to the master port that a new HDLC bit rate is used, the characteristics of the negotiated HDLC channel is vendor specific. The connection establishment and higher layer negotiation is outside the scope of the specification. When the connection is established the “layer 1 start-up timer” shall be cleared.

The slave port shall check that #Z.2.0 is equal in both directions. If it is not equal it shall enter state C. The slave port shall check that at least one of the values #Z.66.0 or #Z.194.0 is equal in both directions. If both differ, it shall enter state D.

Comments:
The master and slave ports exchange information about capabilities and capability limitations resulting in a preferred configuration of the CPRI, including also the vendor specific parts. The negotiation and the corresponding C&M messages are not within the scope of the CPRI specification. The result of the negotiations may require a reconfiguration of the slave or master circuitry. Depending on the degree of change, the start up procedure may have to restart at state B, C or D, with a new set of characteristics (line bit rate, protocol, C&M channel bit rate).

4.5.3.6. State F – Operation

Prerequisites:
The optimum supported C&M channel is established. The use of the vendor specific area is agreed upon.

Description:
Normal operation.

Interpreted control words:
All

Master port actions:
The master port shall check that #Z.2.0 is equal in both directions. If it is not equal it shall enter state C. The master port shall check that at least one of the values #Z.66.0 or #Z.194.0 is equal in both directions. If both differ, it shall enter state D.

Slave port actions:
The slave port shall check that #Z.2.0 is equal in both directions. If it is not equal it shall enter state C. The

slave port shall check that at least one of the values #Z.66.0 or #Z.194.0 is equal in both directions. If both differ, it shall enter state D.

Comments:
In normal operation, the C&M plane has been established and all further setup of HW, functionality, user plane links, IQ format, etc is conducted using procedures outside the scope of the CPRI specification. If the CPRI is subject to a failure state, B is entered. If a reconfiguration is required state D may be entered.

4.5.3.7. State G – Passive Link

Prerequisites:
Layer 1 is synchronized and the protocol is agreed on. The master port does not propose any C&M channel.

Description:
The interface is not carrying the C&M plane

Interpreted control BYTES:
All

Master port actions:
While in this state, the master port shall set the C&M channel bit rates in #Z.66.0 and #Z.194.0 to 0. The master port shall check that #Z.2.0 is equal in both directions. If not equal it shall enter state C.

Slave port actions:
While in this state, the slave port shall set the C&M channel bit rates in #Z.66.0 and #Z.194.0 to the highest available bit rate. The slave port shall check #Z.2.0 is equal in both directions. If it is not equal it shall enter state C. The slave port shall detect any change in the received value #Z.66.0 or #Z.194.0. If at least one value changes it shall enter state D.

Comments:
This state may be entered due to any of the following reasons:

The interface is used for redundancy and does not carry any information at the moment. Further setup is done on the active link.

The interface is used to expand the user plane capacity and its I&Q streams are part of the user plane. Further setup is done on the active link.

As a fallback, the master port may enable the C&M channel by proposing a C&M channel bit rate and the start-up then enters state D. It is therefore important that the slave port transmits a proper C&M channel bit rate.

4.5.4. Transition Description

4.5.4.1. Transition 1

Trigger:
The trigger is out of the scope of the CPRI specification. But it is required for the CPRI circuit initiation to be completed. For the master ports of an RE, this transition is not allowed before one of the slave ports of the RE has been in state E after reset.

A set of available line bit rates, protocol versions and C&M channel bit rates shall be available. This may be the equipment full capabilities or a subset determined by the equipment configuration (manual) or knowledge from previous successful configurations. Such a subset will shorten the time in state B, C and D. Time and frequency references shall be predictive for the master port.

Actions:
None

4.5.4.2. Transition 2

Trigger:
First time the synchronization state HFNSYNC is entered. Received CPRI line bit rate is equal to transmitted CPRI line bit rate.

Actions:
The “layer 1 start-up timer” is set.

4.5.4.3. Transition 3

Trigger:
Protocol is agreed on. First time transmitted #Z.2.0 is equal to received #Z.2.0.

Actions:
None

4.5.4.4. Transition 4

Trigger:
The C&M channel bit rate is agreed on. First time at least one of the two conditions below is fulfilled:

- Received #Z.66.0 is equal to transmitted #Z.66.0, and received #Z.66.0 indicates a valid bit rate.
- Received #Z.194.0 is equal to transmitted #Z.194.0, and received #Z.194.0 indicates a valid bit rate.

4.5.4.5. Transition 5

Trigger:
Out of the scope of the CPRI specification. Application has selected a new C&M channel bit rate set and the C&M channel bit rate is re-setup.

Actions:
The “layer 1 start-up timer” is set.

4.5.4.6. Transition 6

Trigger:
Out of the scope of the CPRI specification. The capability negotiation is accepted by both master and slave ports applications and the present CPRI configuration is considered to be the best available choice.

Actions:
The “layer 1 start-up timer” is cleared.

4.5.4.7. Transition 7

Trigger:
Out of the scope of the CPRI specification. A capability update requiring CPRI capability renegotiation is performed by the applications.

Actions:
None

4.5.4.8. Transition 8

Trigger:
Out of the scope of the CPRI specification. The C&M plane connection is detected lost by the application due to fault or reconfiguration.

Actions:
The “layer 1 start-up timer” is set.

4.5.4.9. Transition 9

Trigger:
Out of the scope of the CPRI specification. The capability negotiation by the application proposes a new CPRI protocol or line bit rate.

Actions:
The transition carries information about the agreed available set of line bit rates, protocol versions and C&M channel bit rates. The “layer 1 start-up timer” is cleared.

4.5.4.10. Transition 10

Trigger:
First time LOS or LOF or received RAI has been found faulty as defined in 4.2.10.

Actions:
The “layer 1 start-up timer” is cleared.

4.5.4.11. Transition 11

Trigger:
The slave or master ports are initiated.

Actions:
The “layer 1 start-up timer” is cleared.

4.5.4.12. Transition 12

Trigger:
First time any of the received C&M channel bit rates in #Z.66.0 or #Z.194.0 is changed while in state E or F.

Actions:
The “layer 1 start-up timer” is set.

4.5.4.13. Transition 13

Trigger:
First time the received protocol version in #Z.2.0 is changed while in state D, E, F or G.

Actions:
The “layer 1 start-up timer” is set.

4.5.4.14. Transition 14

Trigger:
First time the master port has set the #Z.66.0 and #Z.194.0 to indicate that no C&M channel is desired on the interface.

Actions:
The “layer 1 start-up timer” is cleared.

4.5.4.15. Transition 15

Trigger:
First time the master port proposes C&M channel bit rates in at least one of #Z.66.0 or #Z.194.0.

Actions:
The “layer 1 start-up timer” is set.

4.5.4.16. Transition 16

Trigger:
When “layer 1 start-up timer” expires.

Actions:
None

5. Interoperability

5.1. Forward and Backward Compatibility

5.1.1. Fixing Minimum Control Information Position in CPRI Frame Structure

For forward and backward compatibility, the minimum control information position shall be fixed in the CPRI frame in order to find CPRI protocol version correctly. In later versions the position within CPRI hyperframe of the below listed bits shall not be changed:

- Sync and timing (control BYTE: #Z.0.0 in case of 8B/10B line coding or #Z.0.8 in case of 64B/66B line coding)
- Protocol version (control BYTE: #Z.2.0)
- HFN (control BYTE: #Z.64.0)

5.1.2. Reserved Bandwidth within CPRI

Within the CPRI structure some data parts are reserved for future use. These parts may be used in future releases of the CPRI specification to enhance the capabilities or to allow the introduction of new features in a backward compatible way.

Two types of reserved blocks need to be distinguished:

Reserved Bits:

Reserved bits are marked with “r”. This means that a transmitter shall send 0’s for bits marked with “r”, and the receiver shall not interpret bits marked with “r” (transmit: r = 0, receiver: r = don’t care).

Reserved Control Words:

In the current version of the specification 36 control words (subchannels 3 and 8 to 15) of one hyperframe are reserved for future interface protocol extensions. Reserved words are completely filled with reserved bits (reserved bits are marked with “r”).

CPRI reserved data parts shall be used only for protocol enhancements/modifications by the CPRI specification group.

5.1.3. Version Number

The CPRI specification version is indicated by two digits (version A.B). The following text defines the digits’:

- The first digit A is incremented to reflect significant changes (modification of the scope, new section…)
- The second digit B is incremented for all changes of substance, i.e. technical enhancements, corrections, updates, …

5.1.4. Specification Release Version mapping into CPRI Frame

The control BYTE #Z.2.0 indicates the protocol version number, which will be denoted by 1, 2, 3, … The protocol version number will be incremented only when a new specification release version includes changes that lead to incompatibility with previous specification release versions. The simple sequence and the well-defined rule for non-compatibility between different specification release versions allow a simple, efficient and fast start-up procedure. The following table provides the mapping between specification release version and protocol version number.

Table 15: Specification release version and protocol version numbering

Specification release version	Compatible with the following previous specification release versions	Highest available protocol version number (Z.2.0 control BYTE)	
		8B/10B	64B/66B
1.0	-	1	N.A.
1.1	1.0 *	1	N.A.
1.2	1.0 *, 1.1	1	N.A.
1.3	1.0 *, 1.1, 1.2	1	N.A.
2.0	1.0 *, 1.1, 1.2, 1.3	1	N.A.
2.1	1.0 *, 1.1, 1.2, 1.3, 1.4, 2.0	1	N.A.
3.0	1.0 *, 1.1, 1.2, 1.3, 1.4, 2.0, 2.1	1	N.A.
4.0	1.0 *, 1.1, 1.2, 1.3, 1.4, 2.0, 2.1, 3.0	1	N.A.
4.1	1.0 *, 1.1, 1.2, 1.3, 1.4, 2.0, 2.1, 3.0, 4.0	1: scrambling not supported 2: scrambling supported	N.A.
4.2	1.0 *, 1.1, 1.2, 1.3, 1.4, 2.0, 2.1, 3.0, 4.0, 4.1	1: scrambling not supported 2: scrambling supported	N.A.
5.0	1.0 *, 1.1, 1.2, 1.3, 1.4, 2.0, 2.1, 3.0, 4.0, 4.1, 4.2	1: scrambling not supported 2: scrambling supported	N.A.
6.0	1.0 *, 1.1, 1.2, 1.3, 1.4, 2.0, 2.1, 3.0, 4.0, 4.1, 4.2, 5.0	1: scrambling not supported 2: scrambling supported	1
6.1	1.0 *, 1.1, 1.2, 1.3, 1.4, 2.0, 2.1, 3.0, 4.0, 4.1, 4.2, 5.0, 6.0	1: scrambling not supported 2: scrambling supported	1

* The compatibility between V1.0 and the other specification release versions requires the V1.0 receiver to tolerate the /I1/ sequence as specified in section 4.2.7.5.

This table shall be updated when new specification release versions become available.

5.2. Compliance

A CPRI compliant interface application fulfils all following requirements:

- Establishes and maintains a connection between RE and REC by means of mandatory and optional parts of the CPRI specification.
- Establishes and maintains a connection between RE and REC by means of supporting all mandatory parts of CPRI specification.
- Establishes and maintains a connection between RE and REC by means of selecting at least one option out of every option list in the CPRI specification.
- Does not add any additional options in an option list.
- Does not add additional option lists.
- Does not produce errors when passing data between SAP´s in RE and REC.

CPRI module(s) compliance

It is not required that CPRI compatible modules meet the full set of requirements defined in section 4. The performance of the module may be restricted to a subset of the requirements when an application does not require the full performance of the CPRI specification.

For each CPRI compatible module, the vendor shall explicitly declare compliance of the module using the Protocol Implementation Conformance Statement (PICS), available at www.cpri.info.

6. Annex A – Supplementary Specification Details

6.1. Delay Calibration Example (Informative)

This section provides an example for the delay calibration procedure that has been described in Section 4.2.9. The single-hop case is explained first and then the multi-hop case is explained.

In the case of a single-hop configuration the delay between REC and RE (**T12** and **T34**) can be estimated as follows.

Step 1) Measure **T14**, the frame timing difference between the output signal at **R1** and the input signal at **R4**. Assume **<T14>** is the measured value of **T14**.

Step 2) Estimate the round trip delay between REC and RE **<T12+T34>** by subtracting the known value **Toffset** from **<T14>**. **<T12+T34>** = **<T14>** - **Toffset**

Step 3) If the downlink delay (**T12**) and the uplink delay (**T34**) are assumed to be the same, the one way delay can be estimated from the round-trip delay by halving it.

<T12> = **<T34>** = **<T12+T34>** / 2 = (**<T14>** - **Toffset**) / 2

As these two reference points **R1** and **R4** are in the same equipment, REC, it is feasible to measure the **T14** accurate enough to fulfil the requirement (R-21) in Section 7.1.

Of course it may be difficult to measure the timing at **R1** and **R4** directly because the signals at these points are optical or electrical high speed signals, but it is feasible to measure the timing difference somewhere in REC (e.g. before and after the SERDES) and to compensate the internal timing difference between measurement points and **R1**/**R4**.

As it is feasible enough to assume that the REC knows the overall downlink delay (**T2a**) and the uplink delay (**Ta3**) in the RE, the REC is able to estimate the overall delay including the delay between REC and RE by adding **<T12>** and **<T34>**. In case of TDD mode, the computation may require further knowledge of the actual WiMAX frame configuration.

Where,

- **T2a** is the delay from the UMTS frame boundary (UTRA-FDD/E-UTRA) or the WiMAX frame boundary (WiMAX) of the downlink signal at **R2** to the transmit timing at the RE antenna (Ra) of the first IQ sample carried in the corresponding UMTS frame (UTRA-FDD/E-UTRA) or the corresponding WiMAX frame (WiMAX).
- **Ta3** is the delay from the received signal at the RE antenna (Ra) to the UMTS frame boundary (UTRA-FDD/E-UTRA) or the WiMAX frame boundary (WiMAX) at **R3.** The I/Q sample of the corresponding received signal, which is carried as the first I/Q sample in the UMTS frame (UTRA-FDD/E-UTRA) or in the WiMAX frame (WiMAX), is used to measure the delay.

In the case of WiMAX, the delay may vary depending on the IQ mapping method and the position of the IQ sample in a WiMAX frame.

Therefore, the WiMAX frame boundary as defined in section 4.2.8 and the IQ sample, which is carried as the first sample in a WiMAX frame, are selected to define the delay.

In case of WiMAX TDD/E-UTRA TDD, the first IQ sample in a frame may not have valid content (if transmitter or receiver is inactive). In this case the equivalent delay is measured using any other valid IQ sample and the fixed timing relation to the frame.

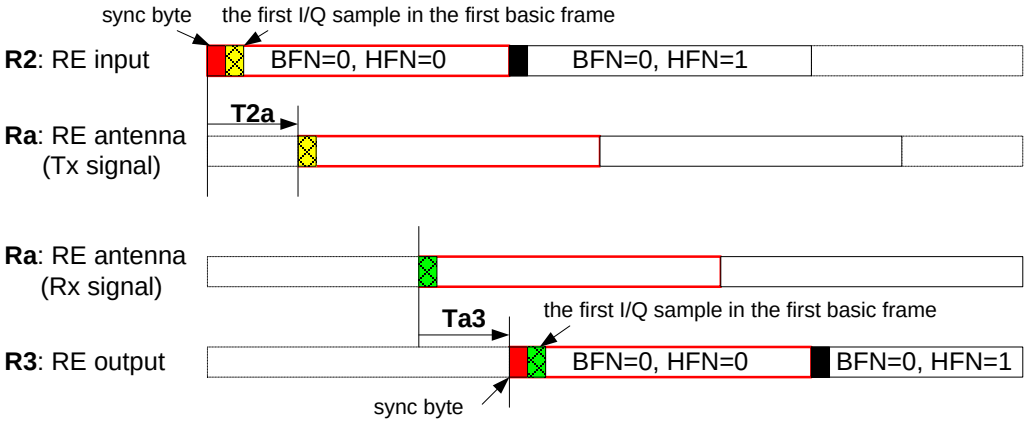


Figure 31: Definition of RE internal delay (UTRA-FDD and E-UTRA)

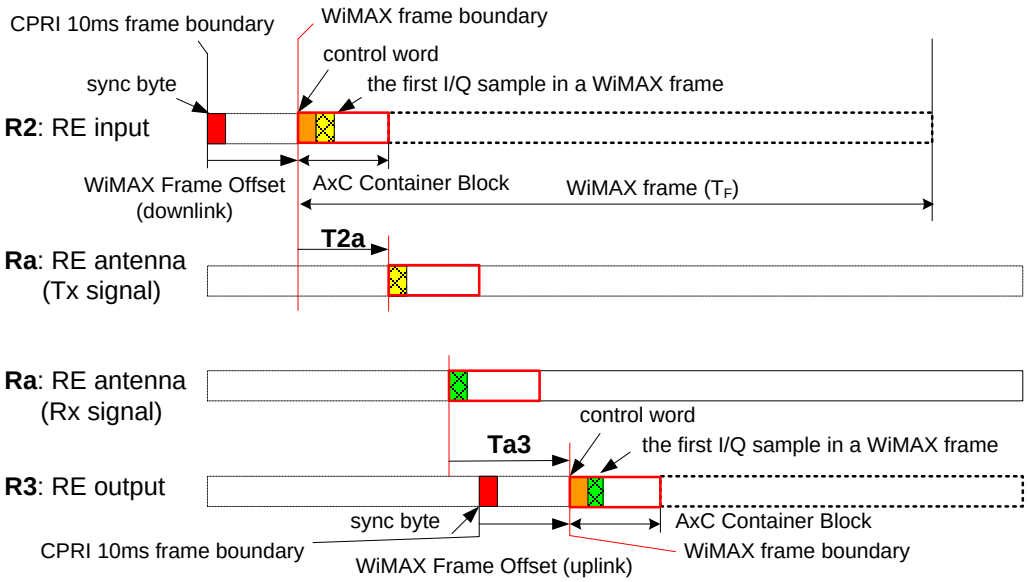


Figure 31A: Definition of RE internal delay (WiMAX FDD only)

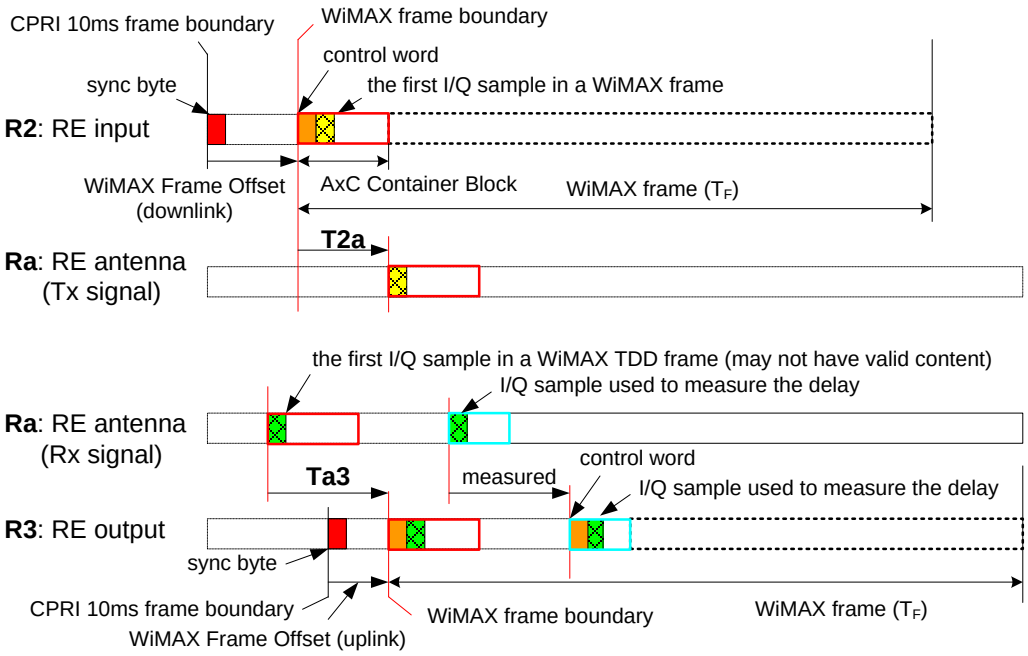


Figure 31B: Definition of RE internal delay (WiMAX TDD only)

In case of a multi-hop configuration[9] the round-trip delay between REC and RE (**T12**+**T34**) can be estimated as follows.

Step 1) Measure **T14**$^{(1)}$, the frame timing difference between the output signal at **R1** and the input signal at **R4**. Assume **<T14**$^{(1)}$**>** is the measured value of **T14**$^{(1)}$.

Step 2) Estimate the end-to-end frame timing difference **T14** by taking into account the difference of frame positions of uplink IQ samples **N**. **<T14>** = **<T14**$^{(1)}$**>** + **N** x T_C,
where T_C is the basic frame length = chip period and N is the sum of all $N^{(i)}$ reported by i-th networking RE (1<=i<=M-1), i.e. $N = \sum_{i=1}^{M-1} N^{(i)}$, "M" is the number of hops.

Step 3) Estimate the round trip delay between REC and RE **<T12+T34>** by subtracting the known value **Toffset** from **<T14>**. **<T12+T34>** = **<T14>** - **Toffset**

As the difference of frame positions of uplink IQ samples **N** is the definite value (no accumulation of measurement error), the accuracy of round-trip delay does not depend on the number of hops.

However, the estimate of the one-way delay is not as simple as in the single-hop case. Dividing **<T12+T34>** by 2 may not introduce the one way delay **<T12>** and/or **<T34>** because the assumption **<T12>** = **<T34>** is no longer feasible as the internal delays in networking REs, **TBdelayDL**$^{(i)}$ and **TBdelayUL**$^{(i)}$, included in **<T12>** and **<T34>** may not be the same for uplink and downlink.

$$T12 = \sum_{i=1}^{M} T12^{(i)} + \sum_{i=1}^{M-1} TBdelayDL^{(i)}$$

$$T34 = \sum_{i=1}^{M} T34^{(i)} + \sum_{i=1}^{M-1} TBdelayUL^{(i)}$$

TBdelayDL$^{(i)}$ does not depend on the link delay so it is a known value for the networking RE.

TBdelayUL$^{(i)}$ depends on the link delay so it has to be measured in the field.

There may be several methods to estimate the one-way delay **T12** and/or **T34**, following is one example to estimate the **T12** and **T34**.

[9] This section describes the multi-hop configuration with networking REs only as an example. The same method may be applied to any other multi-hop configurations including networking REC(s) if the behaviour described in section 4.2.9 is fulfilled.

Step 4) Each networking RE needs to report the internal delays **TBdelayDL$^{(i)}$** and **TBdelayUL$^{(i)}$** to the REC.

Step 5) The REC needs to estimate the one-way delay **T12** and **T34** by using **<T12+T34>** estimated in step 3 and the values {**TBdelayDL$^{(i)}$**} and {**TBdelayUL$^{(i)}$**} (1<=i<=M-1) reported by networking REs as follows:

$$< T12 >= \{< T12 + T34 > + \sum_{i=1}^{M-1} (TBdelayDL^{(i)} - TBdelayUL^{(i)})\} / 2$$

and

$$< T34 >= \{< T12 + T34 > - \sum_{i=1}^{M-1} (TBdelayDL^{(i)} - TBdelayUL^{(i)})\} / 2$$

6.2. Electrical Physical Layer Specification (Informative)

This section and all the following subsections are informative only.

Four electrical variants are recommended for CPRI usage denoted HV (high voltage), LV (low voltage), LV-II (low voltage II) and LV-III (low voltage III) in Figure 32. The HV variant is guided by 1000Base-CX electrical interface specified in Clause 39 of IEEE 802.3 [22], but with 100Ω impedance and adapted to CPRI line bit rates. The LV variant is guided by the XAUI electrical interface specified in Clause 47 of IEEE 802.3 [22], but adapted to CPRI line bit rates. The LV-II variant is guided by Clause 7 of OIF-CEI02.0 [17], but adapted to CPRI line bit rates, and with BER requirement of 10^{-12}. The LV-III variant is guided by 10GBase-KR, defined in IEEE 802.3 [22] clause 72.7 and clause 72.8, but adapted to CPRI line bit rates.

The intention is to be able to reuse electrical designs from 1000BASE-CX, XAUI, OIF-CEI or 10GBase-KR respectively.

All unit intervals are specified with a tolerance of +/- 100 ppm. The worst-case frequency difference between any transmit and receive clock will be 200 ppm. Note that this requirement is only aiming at achieving a data BER of 10^{-12} through the CPRI link. The CPRI clock tolerance is driven by 3GPP requirements (see 3GPP TS 25.104 [8]).

6.2.1. Overlapping Rate and Technologies

Four different technologies may be used for CPRI with an overlap with respect to CPRI line bit rate ranges.

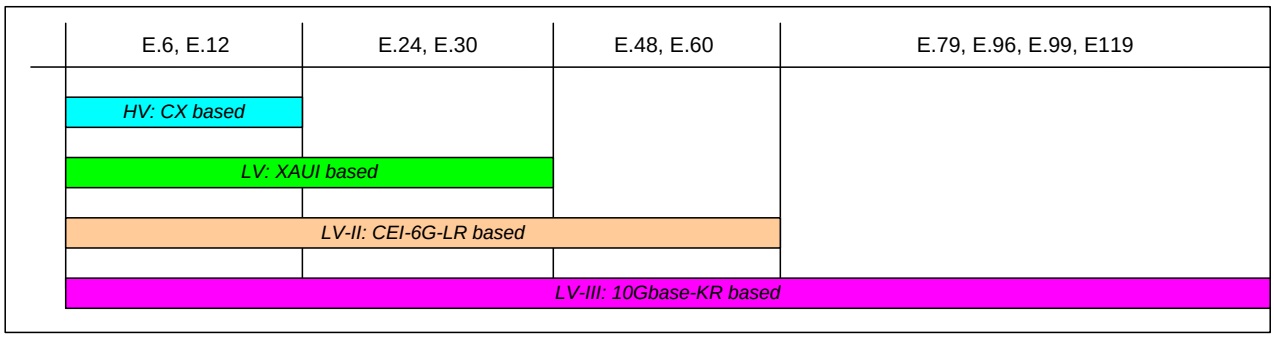


Figure 32: HV, LV, LV-II and LV-III electrical layer 1 usage

Nothing prevents inter-operating the four electrical variants after “bi-lateral” tests. Neither does anything prevent developing a circuit supporting all variants.

6.2.2. Signal Definition

The CPRI link uses differential signalling. Figure 33 defines terms used in the description and specification of the CPRI differential signal pair.

Caution should be taken that some standards and IC data sheet define electrical characteristic with Vdiffpp value, which is twice Vdiff.

The single ended voltage swing is what is measured on one line of the paired differential signal.

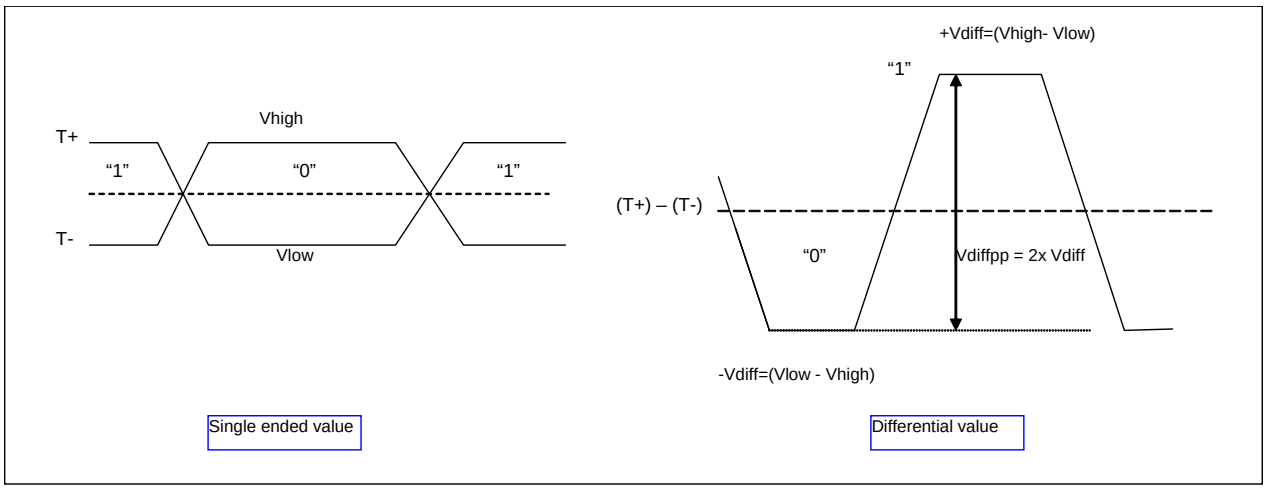


Figure 33: Definition of differential signals of a transmitter or receiver

6.2.3. Eye Diagram and Jitter

Jitter values and differential voltage levels at both Transmitter and Receiver are specified according to the reference eye diagram in Figure 34.

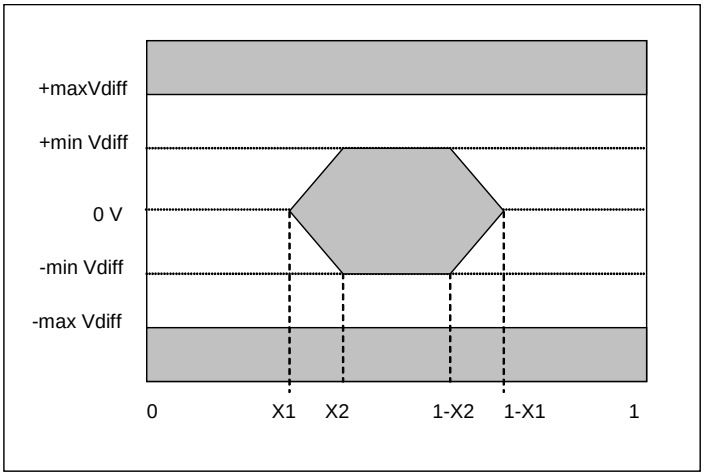


Figure 34: Definition of eye diagram mask

In addition, deterministic and total jitter budget values are specified.

6.2.4. Reference Test Points

Four reference test points are specified:

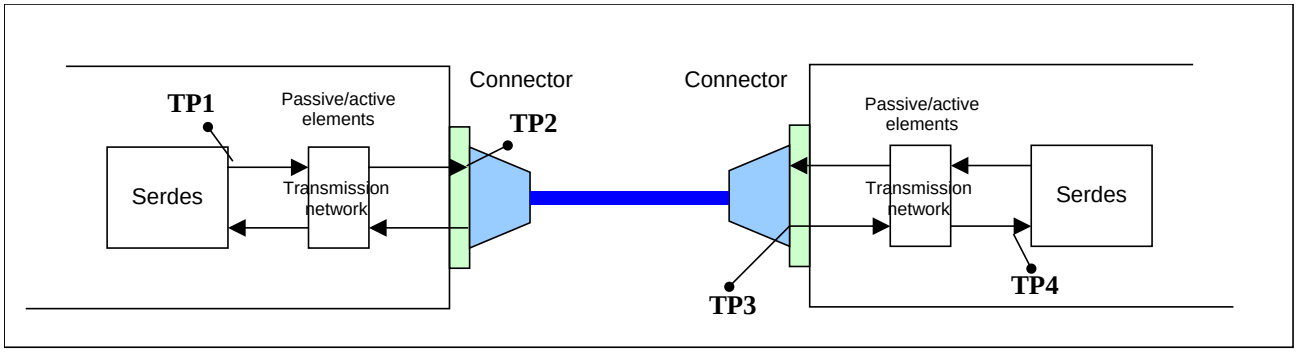


Figure 35: Reference test points

TX and RX requirements are specified at TP1 and TP4 respectively for the Low voltage electrical interface guided by XAUI. The characteristics of the channel between TP1 and TP4 are not included in the CPRI specification.

TX and RX requirement are specified at TP2 and TP3 respectively for the High voltage electrical interface guided by 1000Base-CX. The characteristics of the channel between TP2 and TP3 are not included in the CPRI specification.

TX and RX requirements are specified at TP1 and TP4 respectively for the LV-II electrical interface guided by CEI-6G-LR. The characteristics of channel between TP1 and TP4 which can be designed guided by section 7.3.7 Channel Compliance of OIF-CEI02.0 [17], are not included in the CPRI specification.

TX and RX requirements are specified at TP1 and TP4 respectively for the LV-III electrical interface guided by 10GBase-KR. The characteristics of channel between TP1 and TP4 which can be designed guided by IEEE 802.3 [22] clause 72.8 Interconnect characteristics, are not included in the CPRI specification.

6.2.5. Cable and Connector

Neither cables, nor PCBs, nor connectors are specified for the CPRI.

6.2.6. Impedance

Four options are specified:

- Low Voltage variant: Guided by IEEE 802.3 [22], clause 47. The differential impedance of the channel is 100 Ω.
- High Voltage variant: Guided by IEEE 802.3 [22], clause 39, except that 150 Ω differential impedance is replaced by 100 Ω.
- Low Voltage II variant: Guided by OIF-CEI-02.0, clause 7. The differential impedance of the channel is 100 Ω.
- Low Voltage III variant: Guided by IEEE 802.3 [22], clause 72.7 and Clause 72.8. The differential impedance of the channel is 100 Ω.

6.2.7. AC Coupling

Four options are specified:

- Low Voltage variant: Guided by IEEE 802.3 [22], clause 47. The link is AC coupled at the receiver side.
- High Voltage variant: Guided by IEEE 802.3 [22], clause 39. The link is AC coupled at the receiver side and optionally AC coupled at the transmitter side.
- Low Voltage II variant: Guided by OIF-CEI-02.0, clause 7. The link is AC coupled at the receiver side and optionally AC coupled at the transmitter side.
- Low Voltage III variant: Guided by IEEE 802.3 [22], clause 72.7. The link is AC coupled at the receiver side and optionally AC coupled at the transmitter side.

6.2.8. TX Performances

6.2.8.1. LV TX

The serial transmitter's electrical and timing parameters for E.6.LV, E.12.LV, E.24.LV and E.30LV are stated in this section. All given TX parameters are referred to TP1. The TX parameters are guided by XAUI electrical interface (IEEE 802.3 [22], clause 47).

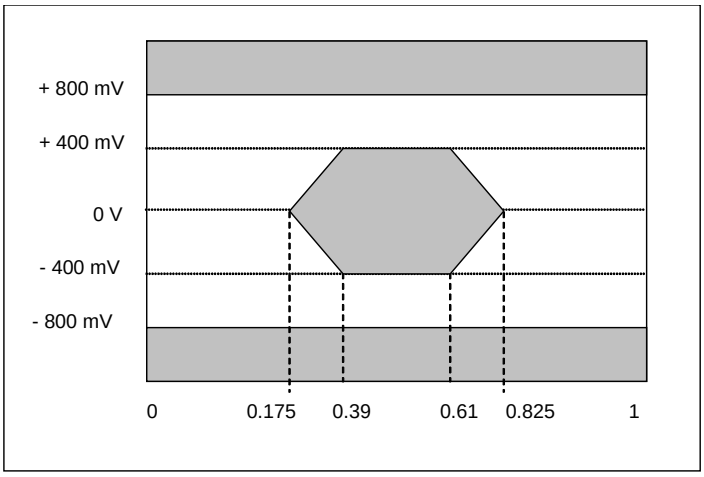


Figure 36: E.6.LV, E.12.LV, E.24.LV, E.30.LV transmitter output mask

Table 16: E.6.LV, E.12.LV, E.24.LV and E.30.LV transmitter AC timing specification

Characteristic	***Symbol***	***Range***		**Unit**	**Notes**
		Min	***Max***		
Output Voltage	Vo	-0.40	2.30	Volts	Voltage relative to common of either signal comprising a differential pair
Differential Output Voltage	V_{DIFFPP}	800	1600	mV,p-p	
Deterministic Jitter	J_D		0.17	UI	
Total Jitter	J_T		0.35	UI	
Unit Interval E.6.LV	UI	1/614.4	1/614.4	µs	+/- 100 ppm
Unit Interval E.12.LV	UI	1/1228.8	1/1228.8	µs	+/- 100 ppm
Unit Interval E.24.LV	UI	1/2457.6	1/2457.6	µs	+/- 100 ppm
Unit Interval E.30.LV	UI	1/3072.0	1/3072.0	µs	+/- 100 ppm

The differential return loss, S11, of the transmitter in each case shall be better than

-10 dB for [CPRI line bit rate/10] < f < 625 MHz, and

-10 dB + 10xlog(f / (625 MHz)) dB for 625 MHz <= f <= [CPRI line bit rate]

The reference impedance for the differential return loss measurement is 100 Ω resistive. Differential return loss includes contribution from SERDES on-chip circuitry, chip packaging and any off-chip components related to the driver. The output impedance requirement applies to all valid output levels.

It is recommended that the 20%-80% rise/fall time of the CPRI-LV Serial transmitter, as measured at the transmitter output, in each case have a minimum value of 60 ps.

It is recommended that the timing skew at the output of a CPRI-LV Serial transmitter between the two signals that comprise a differential pair does not exceed 15 ps.

6.2.8.2. HV TX

The TX electrical and timing parameters for E.6.HV and E.12.HV are stated in this section. All given TX parameters are referred to TP2. The TX parameters are guided by 1000Base-CX (IEEE 802.3 [22], clause 39, PMD to PMI interface).

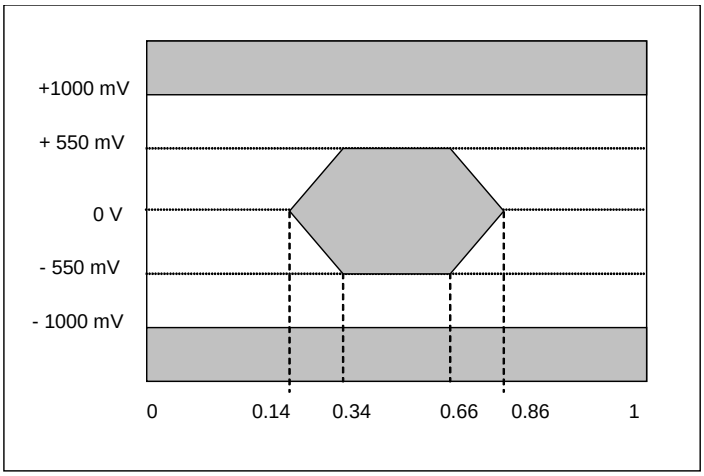


Figure 37: E.6.HV and E.12.HV transmitter mask

Table 17: E.6.HV and E.12.HV transmitter AC timing specification

Characteristic	***Symbol***	***Range***		**Unit**	**Notes**
		Min	***Max***		
Differential Output Voltage	V_{DIFFPP}	1100	2000	mV,p-p	
Rise / Fall time (20% to 80 %)	T_{RF}	85	327	ps	
Deterministic Jitter	J_D		0.14	UI	
Total Jitter	J_T		0.279	UI	
Output skew	S_O		25	ps	
Unit Interval E.6.HV	UI	1/614.4	1/614.4	μs	+/- 100 ppm
Unit Interval E.12.HV	UI	1/1228.8	1/1228.8	μs	+/- 100 ppm

The differential return loss, S11, of the transmitter in each case shall be better than

-15 dB for [CPRI line bit rate/10] < f < 625 MHz, and

-15 dB + 10xlog(f / (625 MHz)) dB for 625 MHz <= f <= [CPRI line bit rate]

The reference impedance for the differential return loss measurement is 100 Ω resistive. Differential return loss includes contribution from SERDES on-chip circuitry, chip packaging and any off-chip components or

transmission lines related to the driver transmission network. The output impedance requirement applies to all valid output levels.

6.2.8.3. LV-II TX

The serial transmitter's electrical and timing parameters for LV-II are stated in this section. All given TX parameters are referred to TP1. The TX parameters are guided by CEI-6G-LR electrical interface (OIF-CEI-02.0 [17], clause 7).

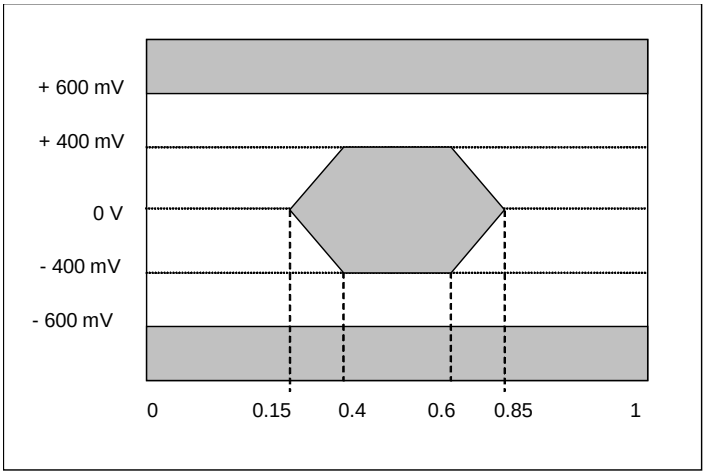


Figure 37A: LV-II transmitter output mask

Table 18A: LV-II transmitter AC timing specification

Characteristic	***Symbol***	***Range***		**Unit**	**Notes**
		Min	***Max***		
Output Voltage	Vo	0.1	1.70	Volts	Voltage relative to common of either signal comprising a differential pair
Differential Output Voltage	VDIFFPP	800	1200	mV,p-p	
Uncorrelated Bounded High Probability Jitter	T_UBHPJ		0.15	UI	
Duty Cycle Distortion	T_DCD		0.05	UI	DCD is only required for line bit rate $\geqslant$ 4.9152Gbps
Total Jitter (Peak-to-Peak)	J_T		0.30	UI	@ 10^{-12} BER
Unit Interval E.6.LV-II	UI	1/614.4	1/614.4	μs	+/- 100 ppm
Unit Interval E.12.LV-II	UI	1/1228.8	1/1228.8	μs	+/- 100 ppm
Unit Interval E.24.LV-II	UI	1/2457.6	1/2457.6	μs	+/- 100 ppm
Unit Interval E.30.LV-II	UI	1/3072	1/3072	μs	+/- 100 ppm
Unit Interval E.48.LV-II	UI	1/4915.2	1/4915.2	μs	+/- 100 ppm
Unit Interval E.60.LV-II	UI	1/6144.0	1/6144.0	μs	+/- 100 ppm

.

The DC differential resistance shall be between 80 and 120Ω.

The differential return loss, S11, of the transmitter in each case shall be better than

-8 dB for 100MHz < f < 0.75* [CPRI line bit rate], and

-8dB + 16.6*log(f / (0.75* [CPRI line bit rate])) dB for 0.75* [CPRI line bit rate] <= f <= [CPRI line bit rate]

The reference impedance for the differential return loss measurement is 100Ω resistive. Differential return loss includes contribution from SERDES on-chip circuitry, chip packaging and any off-chip components related to the driver. The output impedance requirement applies to all valid output levels.

The Common Mode Return Loss of the transmitter in each case shall be better than

-6 dB for 100MHz < f < 0.75* [CPRI line bit rate]

The reference impedance for the common mode return loss is 25Ω.

The recommended minimum differential rise and fall time is 30ps as measured between the 20% and 80% of the maximum measured levels. The maximum differential rise and fall times are defined by the Tx eye diagram. Shorter rise and falls may result in excessive high frequency components and increase EMI and cross talk.

It is recommended that the timing skew at the output of a Serial transmitter between the two signals that comprise a differential pair does not exceed 15 ps.

6.2.8.4. LV-III TX

The serial transmitter's electrical and timing parameters for LV-III are stated in this section. All given TX parameters are referred to TP1. The TX parameters are guided by 10GBase-KR electrical interface (IEEE 802.3 [22], clause 72.7.1).

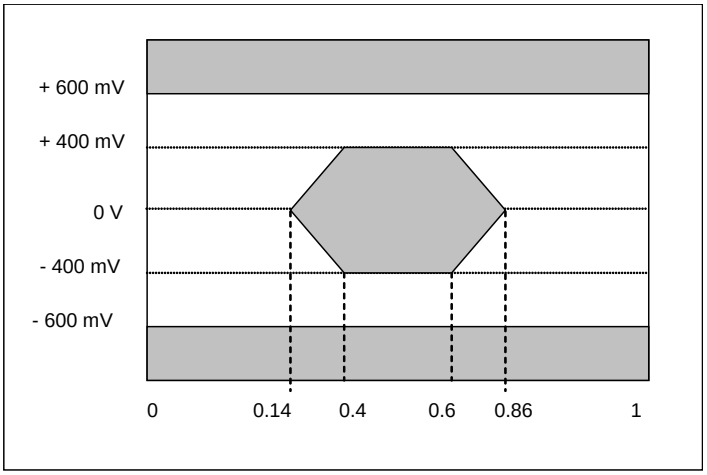


Figure 37B: LV-III transmitter output mask

Table 18B: LV-III transmitter AC timing specification

Characteristic	*Symbol*	*Range*		Unit	Notes
		Min	*Max*		
Common-mode voltage limits	Vo	0	1.90	Volts	
Differential Output Voltage	VDIFFPP	800	1200	mV,p-p	
Deterministic Jitter	T_DJ		0.15	UI	
Duty Cycle Distortion	T_DCD		0.005	UI	DCD ≤ 0.05 UI (4. 9152 ≤ rate < 9.8304 Gbps)
			0.035	UI	DCD ≤ 0.035 UI (9.8304 Gbps ≤ rate)
Random Jitter	T_RJ		0.15	UI	@ 10^{-12} BER
Unit Interval E.24.LV-III	UI	1/2457.6	1/2457.6	µs	+/- 100 ppm
Unit Interval E.30.LV-III	UI	1/3072	1/3072	µs	+/- 100 ppm
Unit Interval E.48.LV-III	UI	1/4915.2	1/4915.2	µs	+/- 100 ppm
Unit Interval E.60.LV-III	UI	1/6144.0	1/6144.0	µs	+/- 100 ppm
Unit Interval E.79.LV-III	UI	1/8110.08	1/8110.08	µs	+/- 100 ppm
Unit Interval E.96.LV-III	UI	1/9830.4	1/9830.4	µs	+/- 100 ppm
Unit Interval E.99.LV-III	UI	1/10137.7	1/10137.6	µs	+/- 100 ppm
Unit Interval E.119.LV-III	UI	1/12165.12	1/12165.12	µs	+/- 100 ppm

The differential return loss, S11, of the transmitter in each case shall be better than

-9 dB for 50MHz <= f <2500MHz, and

-9dB + 12*log(f / 2500MHz) dB for 2500MHz <= f <= 7500MHz

The reference impedance for the differential return loss measurement is 100Ω resistive. Differential return loss includes contribution from SERDES on-chip circuitry, chip packaging and any off-chip components related to the driver. The output impedance requirement applies to all valid output levels.

The Common Mode Return Loss of the transmitter in each case shall be better than

-6 dB for 50MHz <= f <2500MHz

-6dB + 12*log(f / 2500MHz) dB for 2500MHz <= f <= 7500MHz

The reference impedance for the common mode return loss is 25Ω.

The rising and falling edge transition times shall be between 24 ps and 47 ps as measured at the 20% and

80% levels. Shorter rise and falls may result in excessive high frequency components and increase EMI and cross talk.

It is recommended that the timing skew at the output of a serial transmitter between the two signals that comprise a differential pair does not exceed 9 ps.

6.2.8.5. Pre-emphasis and TX-Compliance

Pre-emphasis is allowed by CPRI to overcome data dependent jitter issue. Neither specific pre-emphasis value nor other equalization technique is specified within CPRI.

The output eye pattern of a CPRI transmitter that implements pre-emphasis (to equalize the link and reduce inter-symbol interference) need only comply with the Transmitter Output Compliance Mask when pre-emphasis is disabled or minimized.

For LV and HV variants, Pre-emphasis techniques are to be tested on a bilateral end-to-end basis in between CPRI Nodes.

For LV-II variant, the Pre-emphasis compliance testing is guided by section 2.4.3 Transmitter Interoperability of OIF-CEI02.0 [17]. It shall be verified that the measured eye is equal or better than the calculated eye for the given measurement probability Q (for 10^{-12} BER, Q is 7.035).

For LV-III variant, the Pre-emphasis compliance testing is guided by IEEE 802.3 [22] clause 72.7.1.11 Transmitter output waveform requirements of 10GBase-KR.

6.2.9. Receiver Performances

6.2.9.1. LV RX

The serial receiver electrical and timing parameters for E.6.LV, E.12.LV, E.24.LV and E.30.LV are stated in this section. All given RX parameters are referred to TP4. The RX parameters are guided by XAUI (IEEE 802.3 [22], clause 47).

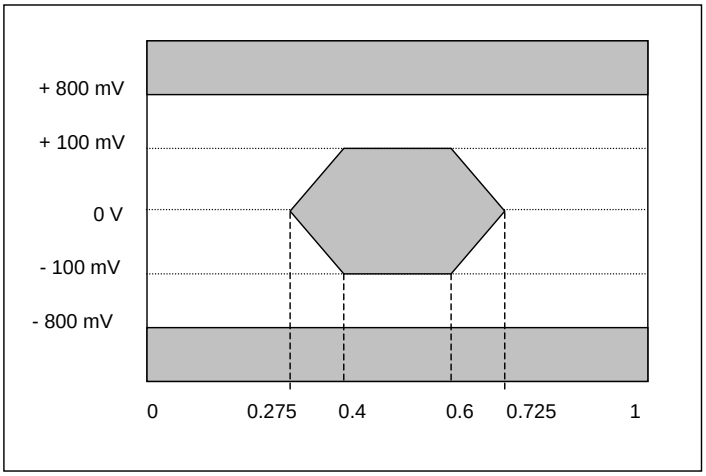


Figure 38: E.6.LV, E.12.LV, E.24.LV and E.30.LV receiver mask

Table 19: E.6.LV, E.12.LV, E.24.LV, and E.30.LV receiver AC timing specification

Characteristic	***Symbol***	***Range***		**Unit**	**Notes**
		Min	***Max***		
Differential Input Voltage	V_{IN}	200	1600	mV,p-p	Measured at receiver
Deterministic Jitter	J_D		0.37	UI	Measured at receiver
Combined Deterministic and Random Jitter	J_{DR}		0.55	UI	Measured at receiver
Total Jitter	J_T		0.65[1]	UI	Measured at receiver
Bit Error Rate	BER		10^{-12}		
Unit Interval E.6.LV	UI	1/614.4	1/614.4	µs	+/- 100 ppm
Unit Interval E.12.LV	UI	1/1228.8	1/1228.8	µs	+/- 100 ppm
Unit Interval E.24.LV	UI	1/2457.6	1/2457.6	µs	+/- 100 ppm
Unit Interval E.30.LV	UI	1/3072.0	1/3072.0	µs	+/- 100 ppm

Note:

1. Total random jitter is composed of deterministic jitter, random jitter and single frequency sinusoidal jitter. The sinusoidal jitter's amplitude and frequency is defined in agreement with XAUI specification IEEE 802.3 [22], clause 47.

Input impedance is defined as 100Ω and is tested by return loss measurement.

Receiver input impedance shall result in a differential return loss better that 10 dB and a common mode return loss better than 6 dB from [CPRI line bit rate/10] to [CPRI line bit rate] frequency. This includes contributions from on chip circuitry, the chip package and any off-chip components related to the receiver. AC coupling components are included in this requirement. The reference impedance for return loss measurements is 100Ω resistive for differential return loss and 25 Ω resistive for common mode.

6.2.9.2. HV RX

The RX electrical and timing parameters for E.6.HV and E.12.HV are stated in this section. All given RX parameters are referred to TP3. The RX parameters are guided by 1000Base-CX (IEEE 802.3 [22], clause 39, PMD to PMI interface).

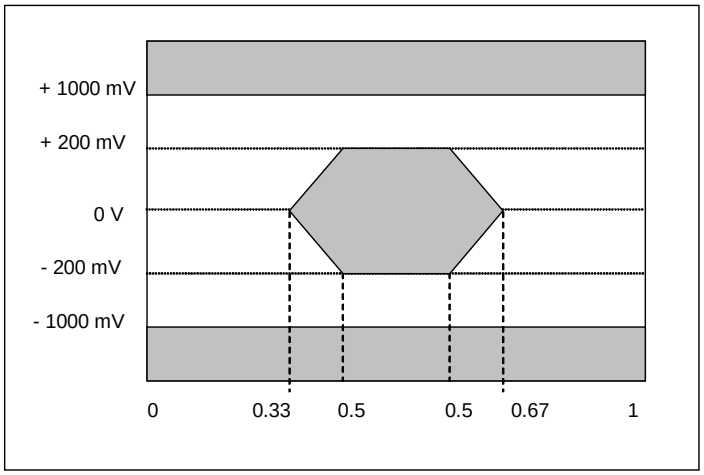


Figure 39: E.6.HV and E.12.HV receiver mask

Table 19Z: E.6.HV and E.12.HV receiver AC timing specification

Characteristic	***Symbol***	***Range***		**Unit**	**Notes**
		Min	***Max***		
Differential Input Voltage	V_{IN}	400	2000	mV,p-p	
Deterministic Jitter	J_D		0.40	UI	
Total Jitter	J_T		0.66	UI	
Differential input skew	S_I		175	ps	
Bit Error Rate	BER		10^{-12}		
Unit Interval E.6.HV	UI	1/614.4	1/614.4	μs	+/- 100 ppm
Unit Interval E.12.HV	UI	1/1228.8	1/1228.8	μs	+/- 100 ppm

Input impedance is defined as 100Ω and is tested by return loss measurement.

Receiver input impedance shall result in a differential return loss better that 15 dB and a common mode return loss better than 6 dB from [CPRI line bit rate/10] to [CPRI line bit rate] frequency. This includes contributions from SERDES on chip circuitry, the chip package and any off-chip components or transmission lines related to the receiver transmission network. AC coupling components are included in this requirement. The reference impedance for return loss measurements is 100Ω resistive for differential return loss and 25 Ω resistive for common mode.

6.2.9.3. LV-II RX

The serial receiver electrical and timing parameters for LV-II are stated in this section. All given RX parameters are referred to TP4. The RX parameters are guided by CEI-6G-LR electrical interface (OIF-CEI-02.0, clause 7).

Table 19A: LV-II receiver characteristic

Characteristic	***Symbol***	***Range***		**Unit**	**Notes**
		Min	***Max***		
Differential Input Voltage	VIN		1200	mV,p-p	Measured at receiver
Differential Resistance	R_Rdin	80	120	Ω	
Differential Input Return Loss 100MHz to 0.75*R_Baud)	R_SDD11		-8	dB	
Differential Input Return Loss (0.75*R_Baud to R_Baud))			16.6	dB/dec	
Common Mode Input Return Loss (100MHz to 0.75 *R_Baud)	R_SCC11		-6	dB	
Unit Interval E.6.LV-II	UI	1/614.4	1/614.4	µs	+/- 100 ppm
Unit Interval E.12.LV-II	UI	1/1228.8	1/1228.8	µs	+/- 100 ppm
Unit Interval E.24.LV-II	UI	1/2457.6	1/2457.6	µs	+/- 100 ppm
Unit Interval E.30.LV-II	UI	1/3072	1/3072	µs	+/- 100 ppm
Unit Interval E.48.LV-II	UI	1/4915.2	1/4915.2	µs	+/- 100 ppm
Unit Interval E.60.LV-II	UI	1/6144.0	1/6144.0	µs	+/- 100 ppm

The differential return loss of the receiver shall be better than

-8 dB for 100MHz < f < 0.75* [CPRI line bit rate], and

-8dB + 16.6*log(f / (0.75* [CPRI line bit rate])) dB for 0.75* [CPRI line bit rate] <= f <= [CPRI line bit rate]

The reference impedance for the differential return loss measurement is 100Ω resistive.

The Common Mode Return Loss of the transmitter in each case shall be better than

-6 dB for 100MHz < f < 0.75* [CPRI line bit rate]

The reference impedance for the common mode return loss is 25Ω.

Jitter tolerance is defined in section 6.2.9.5 Equalization and RX Compliance.

6.2.9.4. LV-III RX

The serial receiver electrical and timing parameters for LV-III are stated in this section. All given RX parameters are referred to TP4. The RX parameters are guided by 10GBase-KR electrical interface (IEEE 802.3 [22], clause 72.7.2).

Table 19B: LV-III receiver characteristic

Characteristic	*Symbol*	*Range*		Unit	Notes
		Min	*Max*		
Differential Input Voltage	VIN		1200	mV,p-p	Measured at receiver
Bit Error Ratio	BER		1.0E-12		
Unit Interval E.24.LV-III	UI	1/2457.6	1/2457.6	µs	+/- 100 ppm
Unit Interval E.30.LV-III	UI	1/3072	1/3072	µs	+/- 100 ppm
Unit Interval E.48.LV-III	UI	1/4915.2	1/4915.2	µs	+/- 100 ppm
Unit Interval E.60.LV-III	UI	1/6144.0	1/6144.0	µs	+/- 100 ppm
Unit Interval E.79.LV-III	UI	1/8110.08	1/8110.08	µs	+/- 100 ppm
Unit Interval E.96.LV-III	UI	1/9830.4	1/9830.4	µs	+/- 100 ppm
Unit Interval E.99.LV-III	UI	1/10137.6	1/10137.6	µs	+/- 100 ppm
Unit Interval E.119.LV-III	UI	1/12165.12	1/12165.12	µs	+/- 100 ppm

The differential return loss of the receiver shall be better than

-9 dB for 50MHz <= f <2500MHz, and

-9dB + 12*log(f / 2500MHz) dB for 2500MHz <= f <= 7500MHz

The reference impedance for the differential return loss measurement is 100Ω resistive.

The Common Mode Return Loss is not specified.

Receiver interference tolerance is defined in IEEE 802.3[22] clause 72.7.2.1.

6.2.9.5. Equalization and RX Compliance

For HV and LV variant, equalization is allowed by CPRI to overcome data dependent jitter issue. No specific equalization technique is specified within CPRI.

For LV-II variant, the Equalization performance testing is not independent, but included in jitter tolerance guided by section 2.4.4 Receiver Interoperability of OIF-CEI02.0 [17].

For LV-III variant, the Equalization performance testing is not independent, but included in receiver interference tolerance guided by IEEE 802.3 [22] clause 72.7.2.1 of 10GBase-KR.

6.2.10. Measurement Procedure

CPRI does not provide means for physical layer conformance testing on chip level or CPRI module level. The measurement procedures shall be seen as recommendations for the chip manufacturers.

6.2.10.1. Low Voltage Option

Since the Low voltage electrical specification are guided by the XAUI electrical interface specified in Clause 47 of IEEE 802.3 [22], the measurement and test procedures shall be similarly guided by Clause 47. In addition, the CJPAT test pattern defined in Annex 48A of IEEE 802.3 [22] restricted to lane 0 is specified as the test pattern for use in eye pattern and jitter measurements. Annex 48B of IEEE 802.3 [22] is recommended as a reference for additional information on jitter test methods.

6.2.10.2. High Voltage Option

Since the High voltage electrical specification are guided by the 1000Base-CX electrical interface specified in Clause 39 of IEEE 802.3 [22], the measurement and test procedures shall be similarly guided by Clause 39, with the impedance value 100 Ω instead of 150 Ω. In addition, the CJPAT test pattern defined in Annex 48A

of IEEE 802.3 [22] restricted to lane 0 is specified as the test pattern for use in eye pattern and jitter measurements. Annex 48B of IEEE 802.3 [22] is recommended as a reference for additional information on jitter test methods.

6.2.10.3. Low Voltage II Option

Since Low voltage II electrical specification are guided by the CEI-6G-LR electrical interface specified in Clause 7 of OIF-CEI-02.0[17], the measurement and test procedures shall be similarly guided by Clause 7.

6.2.10.4. Low Voltage III Option

Since Low voltage III electrical specification are guided by the 10GBase-KR electrical interface specified in Clause 72.7 and Clause 72.8 of IEEE 802.3 [22], the measurement and test procedures shall be similarly guided by Clause 72.7 and Clause 72.8.

6.3. Networking (Informative)

This chapter is informative and aimed at giving examples of network capabilities of an REC and RE assumed in CPRI release 2 or higher. It describes the very basic functionality of the REC and RE to support other topologies than star, e.g. chain, ring or tree topologies.

All functionality described is for informative purpose only and are not mandatory for the REC/RE to implement. Bi-lateral discussions with a system vendor are necessary for REC/RE requirements.

6.3.1. Concepts

RE

The networking capabilities of an RE supporting CPRI release 2 or higher may differ very much between implementations. The functionality is therefore described as an interval between a highly capable RE versus a topology-limited RE. In the following subchapters, the RE functionality is divided into a “simple solution” aiming at using a simplified networking functionality in a chain topology as seen in figure 5A and a more “general solution” aiming at a chain, tree or ring topology as defined in chapter 2.1..

An RE supporting the general solution is characterized by that it may have several slave ports and several master ports.

An RE supporting the simple solution is characterized by that it only has one slave port and one master port which are both using the same line bit rate.

Redundancy

In CPRI release 1, redundancy may exist on hop level by usage of more than one link. In CPRI release 2 or higher, redundancy may also exist on network level. An RE can be connected to the REC through more than one logical connection, each logical connection having its own network path.

6.3.2. Reception and Transmission of SAP_{CM} by the RE

General solution

SAP_{CM} logical connections received on CPRI slave port(s) are switched to CPRI master port(s). The application layer defines the address table used for switching. It is managed in the REC that has full knowledge of the topology and all addresses to all RE’s. The HDLC or Ethernet address can be used to define a table that maps a CPRI port to an address.

Simple solution

For an RE with one CPRI slave port, all messages from the CPRI slave port are forwarded to the master port. Messages received on the CPRI master port are forwarded to the CPRI slave port. The forwarding may be done already at layer 1. The REC must manage the C&M media access in UL (e.g. through a polled protocol).

6.3.3. Reception and Transmission of SAP_{IQ} by the RE

General solution

SAP_{IQ} logical connections received on CPRI slave port(s) are switched to CPRI master port(s). An address table managed by the application layer defines how SAP_{IQ} logical connections shall be switched from one port to another.

Simple solution

For an RE with only one CPRI slave port, all **AxC Containers** from the CPRI slave port are forwarded to the master port. The **AxC Containers** received on the CPRI master port are forwarded to the CPRI slave port. The forwarding may be done already at layer 1.

6.3.4. Reception and Distribution of SAP_S by the RE

General solution

The application layer configures the SAP_S logical connections, i.e. on which slave port to receive the SAP_S and to which master ports to distribute the SAP_S. On the port where SAP_S is received, the RE must fulfil the behaviour as described in section 4.2.9 defined for a slave port. On the ports where the SAP_S is distributed, the RE must fulfil the behaviour in section 4.2.9 defined for a master port.

If the RE loses the slave port for SAP_S due to link failure, the SAP_S is forced to move to another slave port. In order to support chapter 4.2.9, the whole branch of RE's must normally be re-synchronized. The application layer normally manages the re-synchronization.

Simple solution

For an RE with only one CPRI slave port, section 4.2.9 shall be fulfilled. The forwarding of SAP_S to the master port may be done already on layer 1.

6.3.5. Reception and Transmission of CPRI Layer 1 Signalling by the RE

All layer 1 signalling is per hop basis except for the Reset and the SDI. The LOS, LOF and RAI signals are read (in each RE) by the application and signalled to the REC via the application layer.

For the layer 1 Reset, see chapter 4.2.7.6.1.

General solution for SDI

The SDI bit received on a CPRI port is switched to other CPRI port(s) depending on their relation to the port with the SDI set. An address table managed by the application layer defines how the SDI bit shall be switched from one port to another. It is highly recommended that the SAP_{IQ} and SAP_{CM} logical connections are not forwarded from the link where the SDI is set.

Simple solution for SDI

For an RE with only one CPRI slave port, the SDI bit is forwarded to the master port. The forwarding may be done already at layer 1. It is assumed that the IQ user plane and CM messages are forwarded. A SDI bit received on a CPRI master port is read by the application and signalled to the REC via the application layer.

6.3.6. Bit Rate Conversion

An RE is allowed to use different bit rates on its CPRI links, e.g. a high-speed slave port and multiple low-speed master ports.

6.3.7. More than one REC in a radio base station

Up to CPRI release 3 only one REC per base station was considered. Therefore clock/frame synchronization (sections 7.1.5 and 4.2.8) and delay calibration (sections 7.1.6 and 4.2.9) were defined with reference to "the REC". In CPRI release 4 and higher also multiple RECs per base station are considered. In the case of multiple RECs the decision which REC is to be taken for clock reference, is assumed to depend on the individual application. The decision process and the detailed consequences thereof are not described in the CPRI specification.

In the case of multiple RECs some RECs might also have slave ports. In the latter case section 6.3.8 also applies.

6.3.8. The REC as a Networking Element

In CPRI release 4.0 and higher, the REC may be used as a networking element (figure 5D and figure 5E in chapter 2.3). The usage of a networking REC is not fully specified but the following apply.

- Reception and Transmission of SAP_{CM} follow chapter 6.3.2.
- Reception and Transmission of SAP_{IQ} follow chapter 6.3.3.
- Reception and Distribution of SAP_S depends on the topology. A REC may follow chapter 6.3.4 and receive SAP_S from its slave port and distribute it to its master port(s), but may also distribute its own SAP_S to the master port(s).
- Reception and Transmission of CPRI Layer 1 Signalling does not follow chapter 6.3.5. The REC may in general not do a reset when it receives a reset bit on its slave port. The reception and transmission of all CPRI Layer1 Signalling is topology dependent.

6.4. E-UTRA sampling rates (Informative)

Typical sampling rates for E-UTRA are derived for the channel bandwidths listed in Table 5.6-1 of 3GPP TS 36.104 [14].

For each channel bandwidth, the total number of sub-carriers in downlink can be computed by the formula:

$N_{subcarriers} = N_{RB} \times N_{sc}^{RB} + 1$, where N_{sc}^{RB} is equal to 12 (Table 6.2.3-1 of 3GPP TS 36.211 [16])

The size NFFT of the IFFT or FFT operators shall be chosen greater than the number of sub-carriers. Typical values are listed in Table 20.

The sampling frequency f_S can be computed using the formula:

$$f_S = \Delta f \times NFFT,$$

where Δf the sub-carrier separation is equal to 15kHz (Table 6.12-1 of 3GPP TS 36.211 [16]).

Table 20: typical sampling rates for E-UTRA

Channel bandwidth (MHz)	1.4	3	5	10	15	20
Number of subcarriers In downlink	73	181	301	601	901	1201
NFFT	128	256	512	1024	1536, 1024[10]	2048, 1536[10]
Sampling rate (MHz)	1.92	3.84	7.68	15.36	23.04, 15.36[10]	30.72, 23.04[10]
Sampling rate / UMTS chip rate	½	1	2	4	6, 4[10]	8, 6[10]

[10] At some extra cost of complexity in RE channel filtering these values may be used when a higher CPRI link efficiency is required.

6.5. Scrambling (Normative)

The scope of this chapter is limited to 8B/10B line coding.

Scrambling is supported depending on the CPRI line bit rate as shown on Table 21:

Table 21: scrambling support

Line bit rate	Scrambling support	Highest available protocol version number
614.4 Mbit/s	Not supported	1
1228.8 Mbit/s	Not supported	1
2457.6 Mbit/s	Not supported	1
3072.0 Mbit/s	Not supported	1
4915.2 Mbit/s	Recommended	1: scrambling not supported 2: scrambling supported
6144.0 Mbit/s	Recommended	1: scrambling not supported 2: scrambling supported
9830.4 Mbit/s	Recommended	1: scrambling not supported[11] 2: scrambling supported

6.5.1. Transmitter

The scrambler used is a side stream scrambler as shown in Figure 40. The scrambling sequence is constructed using the primitive (over GF(2)) polynomial $P(X) = 1+X^{28}+X^{31}$.

The scrambling sequence c_i (i= 0, 1,…, 256*16*T-1) is constructed as:

- Initial conditions are defined by a 31-bit vector (the seed of the scrambler: c_0,..c_{30}). The choice of the seed is outside the scope of the CPRI specification. A seed with all bits equal to '0' is not precluded and allow disabling the scrambling operation.
- Recursive definition of subsequent symbols: $c_{i+31} = c_i + c_{i+3}$ modulo 2 for $i \geq 0$
  c_i bit is the generated bit in time sequence i of the serial pseudorandom code generator (c_0 is the first outgoing bit).
- At each bit period, the shift registers are advanced by one bit and one new bit is generated.
- At the beginning of each hyperframe the scrambler state is reset with the seed value (c_0..c_{30}). Hence, the c_i sequence period is 256*16*T.

The scrambling sequence generator is followed by a serial to parallel function. The input of this function is the c_i sequence. The output is a byte sequence C_n (n= 0, 1,…, 512*T-1) defined by:

$$C_n = (c_{8n} \text{ (LSB)}, c_{8n+1}, \ldots, c_{8n+7} \text{ (MSB)}) \text{ for } 0 \leq n < 512*T$$

Byte sequence C'_n (n= 0, 1,…,512*T-1) is defined by following formula to prevent control BYTES #Z.X.Y with index Y ≤ 1 of subchannel Ns=0 (X= 0, 64, 128 and 192) and subchannel Ns=2 (X= 2, 66, 130 and 194) to be scrambled:

if $n \in \{0;1;4T; 4T+1; 128T; 128T+1; 132T; 132T+1; 256T; 256T+1; 260T; 260T+1; 384T; 384T+1; 388T; 388T+1\}$

$C'_n = 0$

[11] At 9830.4 Mbps line bit rate scrambling is strongly recommended.

else

$$C'_n = C_n$$

where n= 2*T*X + W*T/8 + Y = 0, 1,..., 512*T-1.

The input of the 8B/10B encoder is the result of a bit wise XOR operation between the byte #Z.X.W.Y[12] and $C'_{2TX+WT/8+Y}$

The timing relation between the byte #Z.X.W.Y and C'_n is shown in Figure 41.

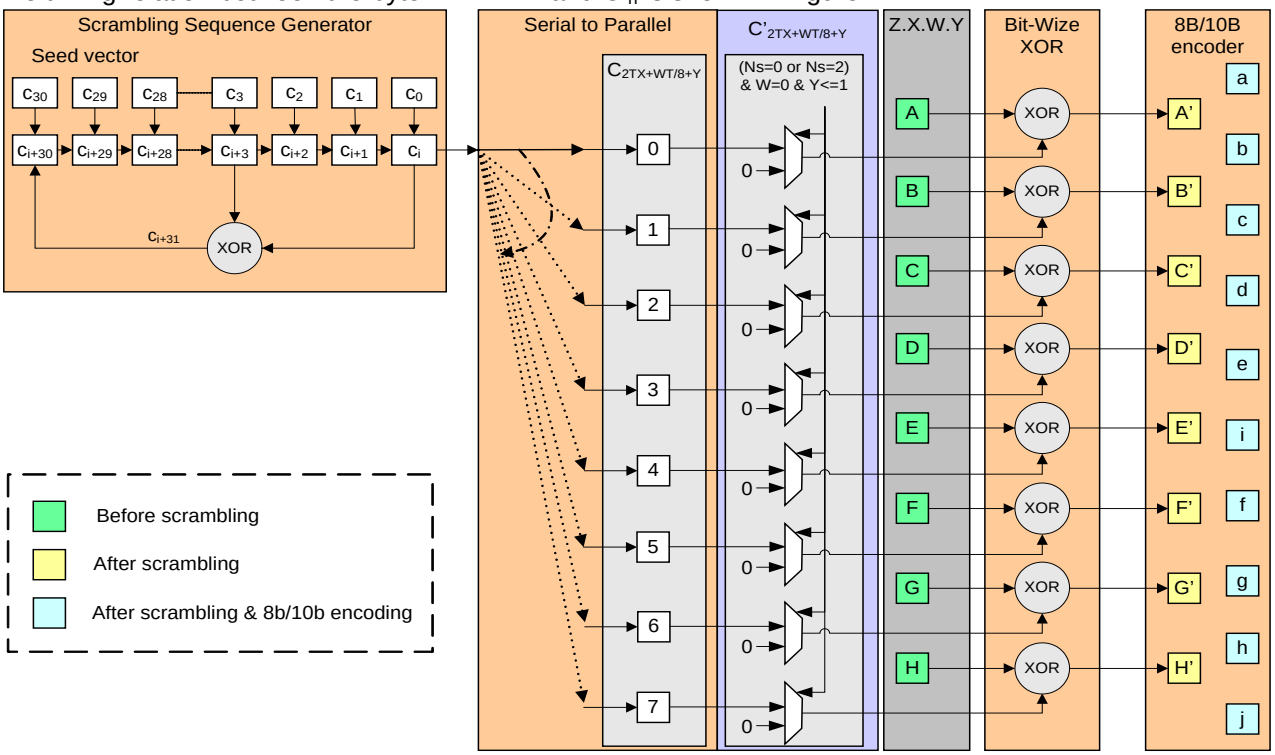
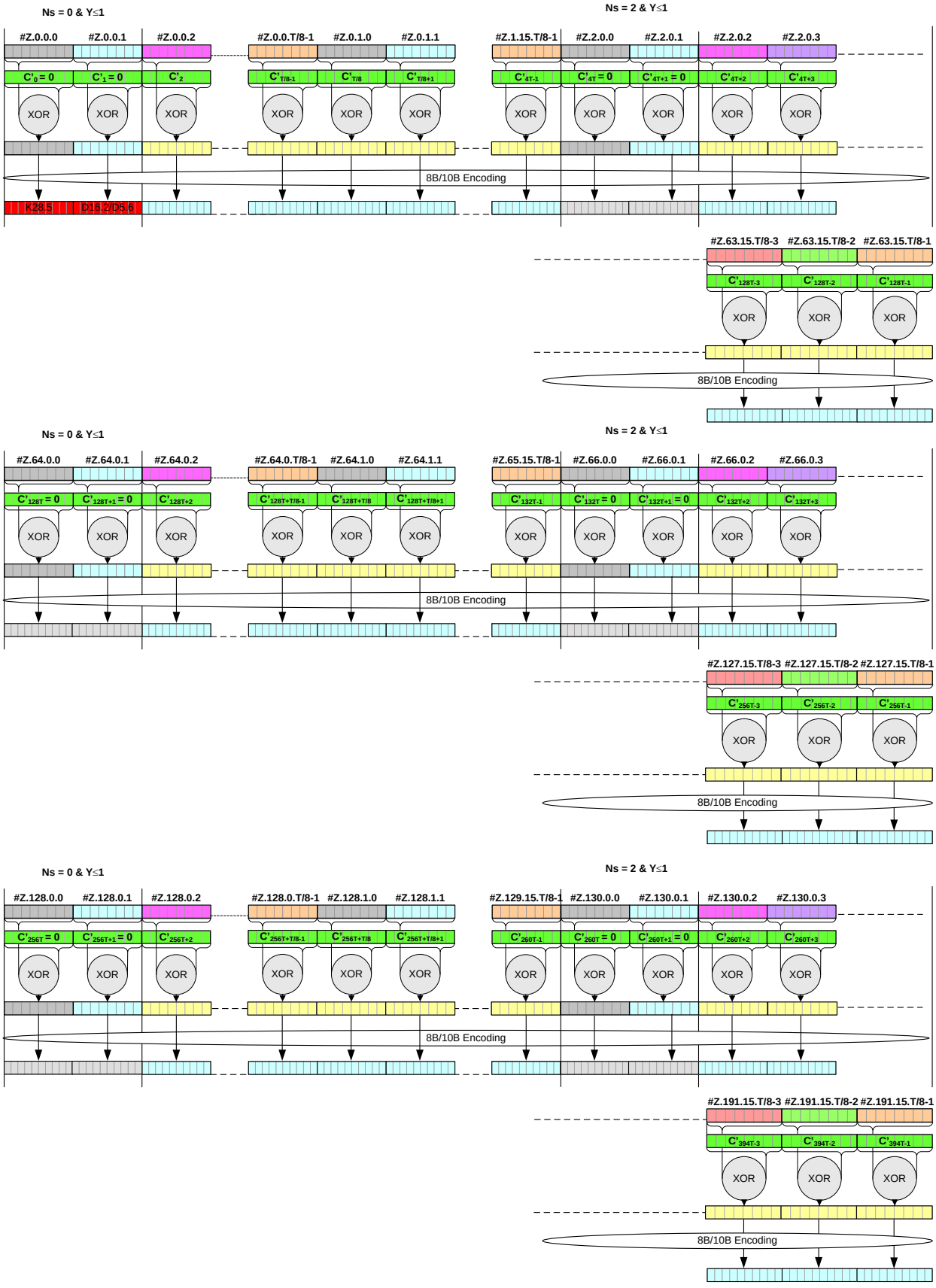


Figure 40: Scrambling function

[12] refer to section 4.2.7.1.2 for more details


Ns = 0 & Y≤1
Ns = 2 & Y≤1
#Z.0.0.0
#Z.0.0.1
#Z.0.0.2
#Z.0.0.T/8-1
#Z.0.1.0
#Z.0.1.1
#Z.1.15.T/8-1
#Z.2.0.0
#Z.2.0.1
#Z.2.0.2
#Z.2.0.3
C'0 = 0
C'1 = 0
C'2
C'T/8-1
C'T/8
C'T/8+1
C'4T-1
C'4T = 0
C'4T+1 = 0
C'4T+2
C'4T+3
XOR
8B/10B Encoding
K28.5
D16.2/D5.6
#Z.63.15.T/8-3
#Z.63.15.T/8-2
#Z.63.15.T/8-1
C'128T-3
C'128T-2
C'128T-1
Ns = 0 & Y≤1
Ns = 2 & Y≤1
#Z.64.0.0
#Z.64.0.1
#Z.64.0.2
#Z.64.0.T/8-1
#Z.64.1.0
#Z.64.1.1
#Z.65.15.T/8-1
#Z.66.0.0
#Z.66.0.1
#Z.66.0.2
#Z.66.0.3
C'128T = 0
C'128T+1 = 0
C'128T+2
C'128T+T/8-1
C'128T+T/8
C'128T+T/8+1
C'132T-1
C'132T = 0
C'132T+1 = 0
C'132T+2
C'132T+3
#Z.127.15.T/8-3
#Z.127.15.T/8-2
#Z.127.15.T/8-1
C'256T-3
C'256T-2
C'256T-1
Ns = 0 & Y≤1
Ns = 2 & Y≤1
#Z.128.0.0
#Z.128.0.1
#Z.128.0.2
#Z.128.0.T/8-1
#Z.128.1.0
#Z.128.1.1
#Z.129.15.T/8-1
#Z.130.0.0
#Z.130.0.1
#Z.130.0.2
#Z.130.0.3
C'256T = 0
C'256T+1 = 0
C'256T+2
C'256T+T/8-1
C'256T+T/8
C'256T+T/8+1
C'260T-1
C'260T = 0
C'260T+1 = 0
C'260T+2
C'260T+3
#Z.191.15.T/8-3
#Z.191.15.T/8-2
#Z.191.15.T/8-1
C'394T-3
C'394T-2
C'394T-1

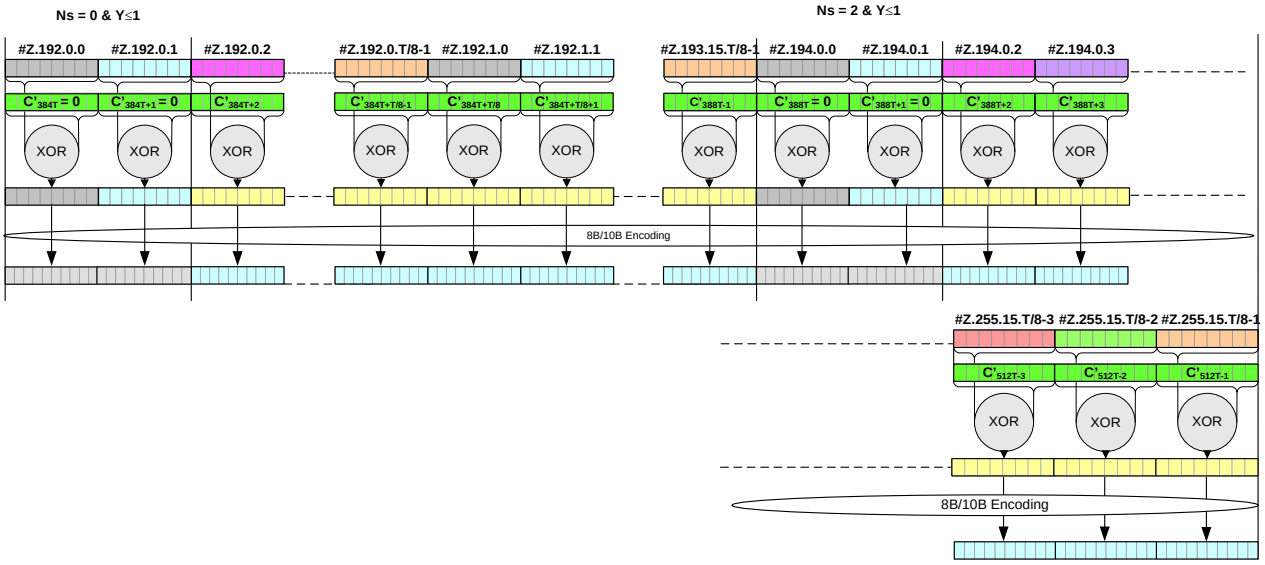


Figure 41: Scrambling of bytes #Z.X.W.Y in hyperframe Z

6.5.2. Receiver

A receiver supporting protocol version 2 shall be capable of receiving data scrambled by the scrambling function described in section 6.5.1 for any seed value.

The receiver shall use at least 31 bits in the control BYTES #Z.0.2 to #Z.0.(T/8-1) to retrieve the scrambling sequence of the transmitter in order to generate the descrambling sequence.

Once the above operation is achieved, the receiver shall periodically check the descrambling sequence with the incoming data, by sampling at least 31 bits of the descrambled control BYTES #Z.0.2, to #Z.0.(T/8-1) known to be 50h (see 4.2.10.3.1)

6.6. GSM sampling rates (Informative)

GSM normal symbol rate is 1625/6 ksymb/s (i.e. approximately 270.833 ksymb/s), see chapter 2.1 of 3GPP TS 45.004 [24]. GSM higher symbol rate is 325 ksymb/s, see chapter 5.1 of 3GPP TS 45.004 [24].

It is recommended to do a re-sampling of the GSM IQ samples according to Table 22 or Table 23 to transfer them on the CPRI-link.

Table 22: Typical sampling rates for GSM (multiple of symbol rate)

GSM symbol rate	Normal	High
ksymb/s	1625/6	325
Re-sampling factor	1, 6, 12	1, 5, 10
Sampling rate (kHz)	1625/6, 1625, 3250	325, 1625, 3250

Table 23: Typical sampling rates for GSM (multiple or sub-multiple of the UTRA-FDD chip rate)

GSM symbol rate	Normal	High
ksymb/s	1625/6	325
Re-sampling factor	1152/325, 2304/325, 4608/325	960/325, 1920/325, 3840/325
Sample rate (kHz)	960, 1920, 3840	960, 1920, 3840
Sampling rate / UMTS chip rate	¼ , ½, 1	¼, ½, 1

6.7. 64B/66B line coding (Normative)

64B/66B line coding is relying on the 10GBase-R PCS block defined in the IEEE 802.3 [22], clause 49.

6.7.1. 64B/66B Supported format

For 64B/66B line coding 3 formats from the IEEE 802.3 [22], Figure 49–7 (64B/66B block formats) are used. These three formats are:

- Control block format with Terminate Control Character
- Control block format with Start Control Character
- Data block format

The 10GBASE-R PCS encodes the start and terminate control characters implicitly by the block type field.

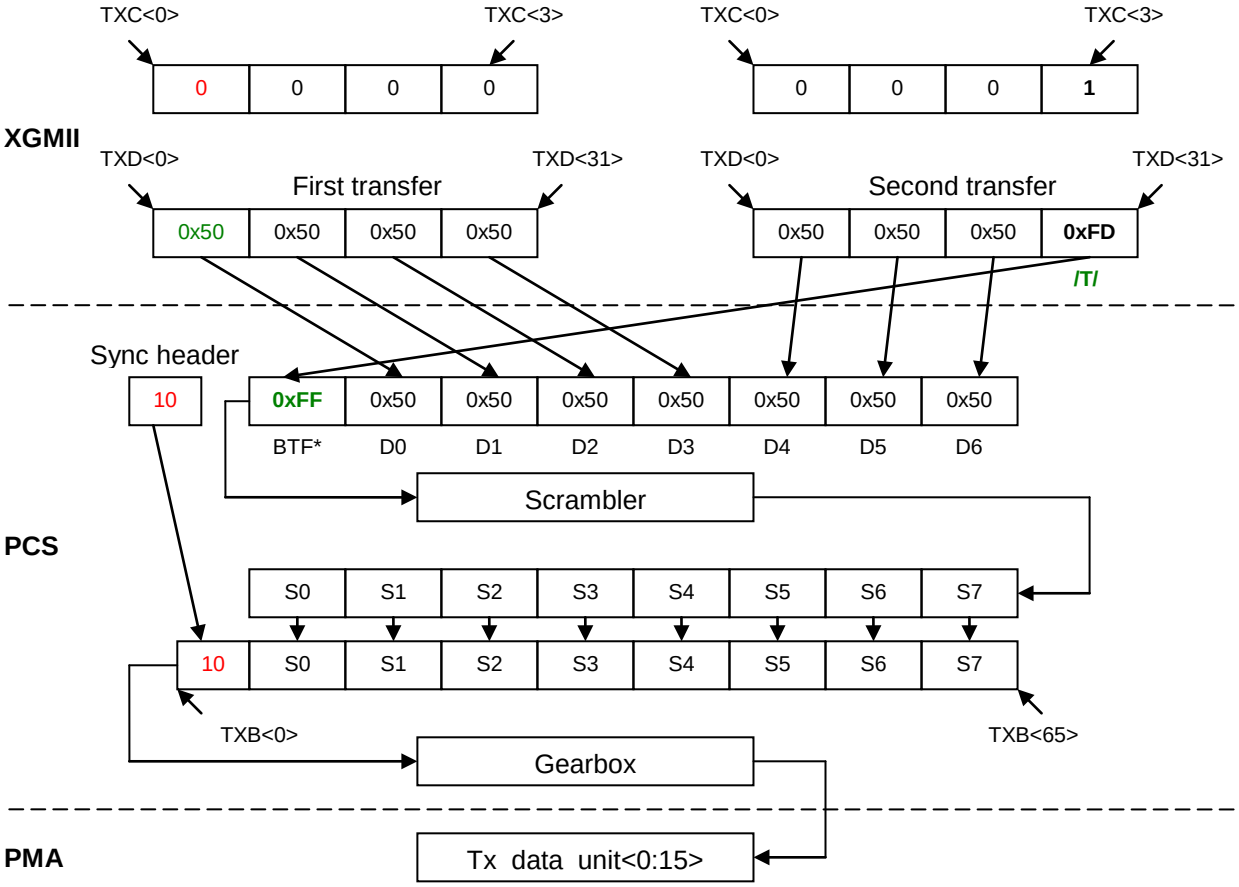
Table 24: 64B/66B Block formats

Input Data	**Sync**	**Block Payload**							
Bit Position: / Data Block Format:	0 1	2.. 9	10..17	18..25	26..33	34..41	42..49	50..57	58..65
$D_0D_1D_2D_3/D_4D_5D_6D_7$	0 1	D0	D1	D2	D3	D4	D5	D6	D7
Control Block Formats:		Block Type Field							
$D_0D_1D_2D_3/D_4D_5D_6T_7$	1 0	0xFF	D0	D1	D2	D3	D4	D5	D6
$S_0D_1D_2D_3/D_4D_5D_6D_7$	1 0	0x78	D1	D2	D3	D4	D5	D6	D7

6.7.2. Control block format with Terminate Control Character

The /T/ character will be positioned in the last 8 bits of the 64 bits.

An example of **/T/** assertion (TXC<3> = 1 & TXD<31:24> = 0xFD) is shown in bold in Figure 42.



*BTF = Block Type Field

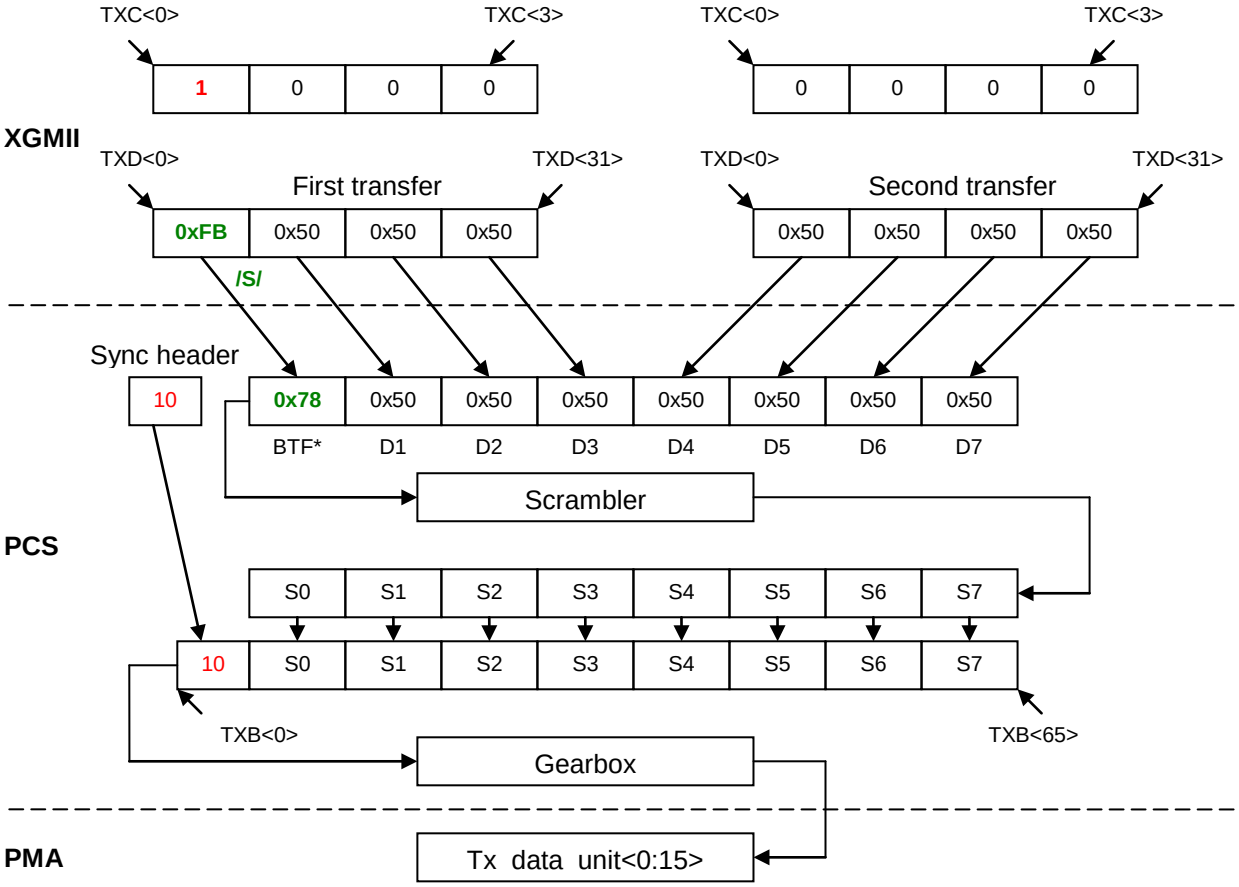
Figure 42: Terminate Control Block at XGMII and PCS levels

As TxC<3:0> doesn't remain at zero, the Sync header changes to "10" instead of "01" to indicate that there is one control character in the payload. The Block Type Field (0xFF) is the first byte of the hyperframe and is positioned in the first 8 bits of the first 64 bits of the hyperframe and aligned with the 64B/66B line coding scheme.

6.7.3. Control block format with Start Control Character

The /S/ character will be positioned in the first 8 bits of the 64 bits.

An example of ***/S/*** assertion (TXC<0> = 1 & TXD<7:0> = 0xFB) is shown in bold in Figure 43.



*BTF = Block Type Field

Figure 43: Start Control Block at XGMII and PCS levels

As TxC<3:0> doesn't remain at zero, the Sync header changes to "10" instead of "01" to indicate that there is one control character in the payload. The Block Type Field (0x78) is the ninth byte of the hyperframe and is positioned in the first 8 bits of the second block of 64 bits of the hyperframe and aligned with the 64B/66B line coding scheme.

6.7.4. Data Block Format

In case of Data transmission, data are grouped by pack of 8 bytes, these 64 bits are scrambled and the bit sequence '01' is added to form the 66 bits sequence.

An example of 64B/66B data block encoding is shown in Figure 44.

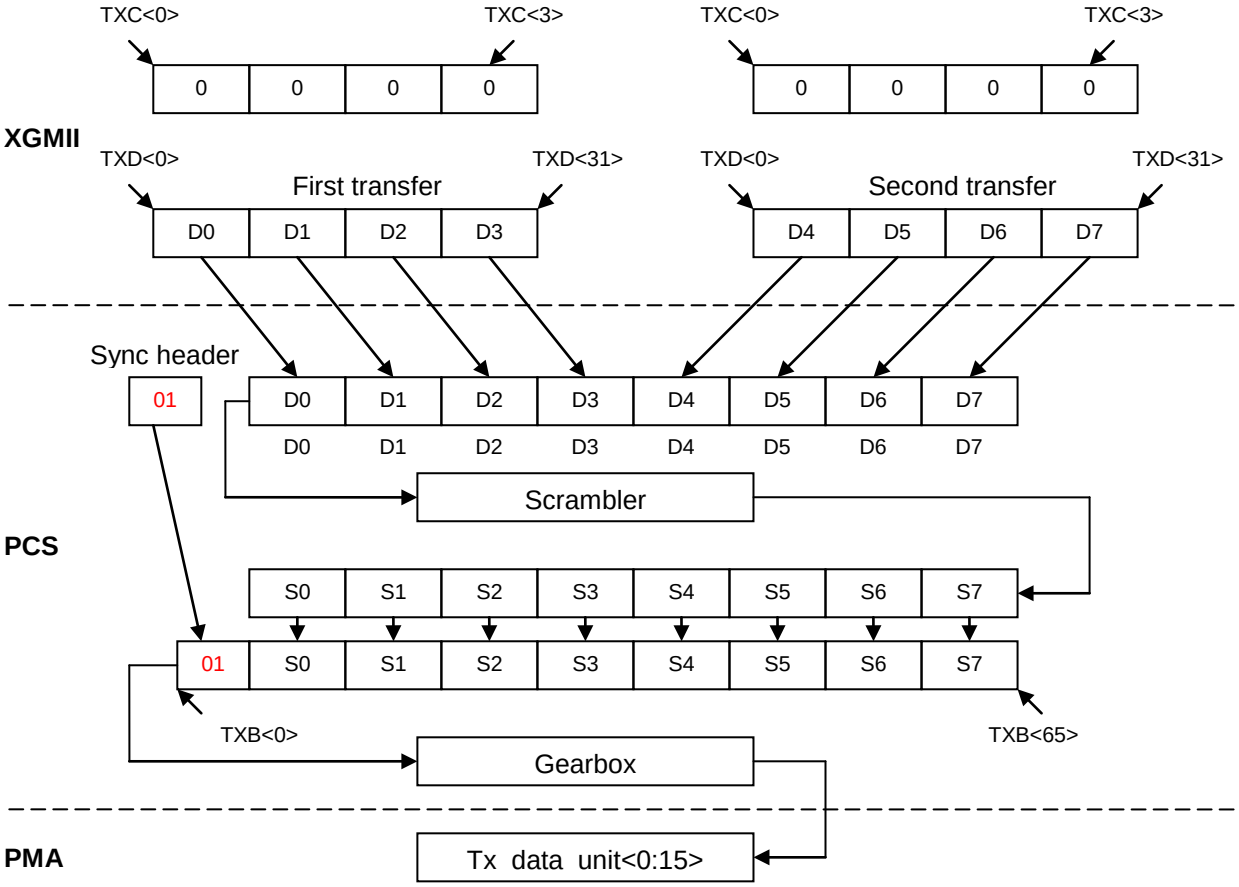


Figure 44: Data block at XGMII and PCS levels

6.7.5. 64B/66B Scrambling

For 64B/66B line coding the scrambling used is defined in the IEEE 802.3 [22], clause 49 and doesn't correspond to the CPRI scrambling defined in section 6.5.

6.8. Additions to line bit rate auto-negotiation (informative)

6.8.1. General recommendation for line bit rate auto-negotiation

The general recommendation for a base station vendor is to limit the available common set of line bit rates for the initial start-up procedure to a maximum of 4 line bit rate options for all RECs and REs. When the state machine reaches state E during initial start-up, a reconfiguration to a final line bit rate can be done using transition 9 of the start-up procedure.

6.8.2. Situation with more than 4 line bit rates for initial start-up

In rare scenarios there might be a hanging-up in state B of the start-up procedure as described in section 4.5.3.2. These rare hanging-up scenarios are always with more than 4 line bit rate options in the available set for the round robin sequence in the master port, and require certain relations between intervals T1 and T1' in master port and slave port, respectively.

6.8.2.1. Example of a hanging-up scenario

This hanging-up scenario assumes fully synchronized[13] intervals between the master port and the slave port:

- T1 = 1 second
- T1' = 4*T1
- Master port set: {5,4,3,2,1}, **5 line bit rate options**
- Slave port set: {8,7,6,5,1}, **5 line bit rate options**
- common set of line bit rate options: {5,1}, **2 line bit rate options**

The timing as shown in Figure 45 indicates that the common line bit rate options will never meet in an overlapping time interval.

time interval	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
master port line rate option	5	4	3	2	1	5	4	3	2	1	5	4	3	2	1	5	4	3	2	1
slave port line rate option	1				8				7				6				5			

Figure 45: Example scenario which leads to hanging-up in state B

6.8.2.2. Examples for vendor specific means

6.8.2.2.1. Example 1 – to be applied on the master port side only

The 1st step is to detect this hanging-up. This may be achieved by either a vendor specific timer or by counting the number of unsuccessful round robin cycles.

The 2nd step may be to restrict the set of available line bit rates in the master port to 4 and then to enter state B of the start-up procedure again.

3rd step (optional, only if the 2nd step is not successful): a different set of 4 available line bit rates in the master port is chosen and then state B of the start-up procedure is entered again.

6.8.2.2.2. Example 2 – to be applied on the master port side only

The 1st step is to detect this hanging-up. This may be achieved by either a vendor specific timer or by counting the number of unsuccessful round robin cycles.

The 2nd step may be to wait before state B is re-entered only on the master port side.

The 1st and the 2nd steps may be repeated several times, probably with different durations of the waiting time.

[13] Even if T1 and T1' are not exactly synchronized but very close T1'≈4*T1 then the state B might take too long for a practical application

7. Annex B - Input Requirements for the CPRI Specification (Informative)

This chapter provides input requirements for the development of the CPRI specification. The requirements are to be met by the CPRI specification, and will be used as a baseline for future enhancements of the CPRI specification. Note that this chapter does not specify the requirements on a CPRI compliant module (see chapter 5.2) but expresses the superset of requirements for an interface from all expected applications using the CPRI.

7.1. Interface Baseline

7.1.1. Supported Radio Standards

The interface shall support transmission of all necessary data between REC and RE in both directions for a radio base station consisting of one REC and one or more REs compliant to the following radio standards:

Requirement No.	Requirement Definition	Requirement Value	Scope
R-1	Supported Radio Standards and Releases	3GPP UTRA FDD, Release 10, March 2012	Logical connection
		WiMAX Forum Mobile System Profile Release 1.5 Approved Specification (2009-08-01)	
		3GPP E-UTRA, Release 10, March 2012	
		3GPP GSM/EDGE Radio Access Network, Release 10, March 2011	

The support of other standards is not required in this release of the CPRI specification, but the future use of the interface for other standards shall not be precluded.

7.1.2. Operating Range

The interface shall support a continuous range of distances (i.e., cable lengths) between master and slave ports. The minimum required range is defined by the cable length in the following table:

Requirement No.	Requirement Definition	Requirement Value	Scope
R-2	Cable length (lower limit)	0 m	Link
R-3	Cable length (upper limit)	>10 km	Link

The interface shall support one cable between master and slave with separate transmission media (e.g., optical fibres) for uplink and downlink.

7.1.3. Topology/Switching/Multiplexing

The interface shall support the following networking topologies:

Requirement No.	Requirement Definition	Requirement Value	Scope
R-4	Topology	Star topology, Chain topology, Tree topology, Ring topology	Radio base station system

The support of other topologies is not required in this release of the specification, but the use of the interface in other topologies shall not be precluded.

The interface shall support multiple hops when used in a networking configuration:

Requirement No.	Requirement Definition	Requirement Value	Scope
R-4A	Maximum number of hops in a logical connection	At least 5 hops	Logical connection

One RE may support several ports to fit in the different topologies but at least one is a slave port:

Requirement No.	Requirement Definition	Requirement Value	Scope
R-4B	Number of ports per RE	RE may support more than one CPRI port	Node

Requirement No.	Requirement Definition	Requirement Value	Scope
R-4C	Number of slave ports per RE	RE shall support at least one CPRI slave port	Node

A logical connection may use a multi-hop connection composed of links with different line bit rates.

Requirement No.	Requirement Definition	Requirement Value	Scope
R-4D	One logical connection may consist of successive hops with different link numbers and line bit rates.	N/A	Logical connection

It shall be possible to use a link as a redundant link in any network topology.

Requirement No.	Requirement Definition	Requirement Value	Scope
R-4E	A link may be used as a redundant link in any network topology.	N/A	Link

It shall be possible to mix different Radio Standards on a link.

Requirement No.	Requirement Definition	Requirement Value	Scope
R-4F	Different Radio Standards may be mixed on a link.	N/A	Link

7.1.4. Bandwidth/Capacity/Scalability

7.1.4.1. Capacity in terms of Antenna-Carriers

The capacity of one logical connection shall be expressed in terms of UTRA-FDD/E-UTRA-antenna-carriers (abbreviation: “antenna-carrier” or “AxC”). One UTRA-FDD/E-UTRA-antenna-carrier is the amount of digital baseband (IQ) U-plane data necessary for either reception or transmission of one UTRA-FDD/E-UTRA carrier at one independent antenna element. One antenna element is typically characterized by having exactly one antenna connector to the RE.

CPRI shall be defined in such a way that the following typical NodeB configurations can be supported:

- 1 RE supports one sector
    - Up to 4 carriers x 1 antenna per RE (e.g. 6 REs for 3 sectors)
    - Up to 4 carriers x 2 antennas per RE (e.g. 3 REs for 3 sectors)
    - Up to 2 component carriers[14] x 8 antennas per RE (E-UTRA Rel-10 and later)
    - Up to 5 component carriers[14] x 2 antennas per RE (E-UTRA Rel-10 and later)
    - Any combination of “up to 5 component carriers[14]” x “up to 8 antennas” per RE (E-UTRA Rel-10 and later)
- 1 RE supports 3 sectors
    - From 1 to 4 carriers x 2 antennas x 3 sectors per RE

[14] A component carrier is defined by 3GPP to achieve wider bandwidth by carrier aggregation (3GPP TS 36.300 [25]).

Therefore, the following number of AxC shall be supported by the CPRI specification:

Requirement No.	Requirement Definition	Requirement Value	Scope
R-10[15]	Number of antenna carriers per logical connection for UTRA FDD/E-UTRA	1..40	Logical connection

7.1.4.2. Required U-plane IQ Sample Widths

The IQ sample widths supported by the CPRI specification shall be between 4 and 20 bits for I and Q in the uplink and between 8 and 20 bits in the downlink.

Requirement No.	Requirement Definition	Requirement Value	Scope
R-11	Minimum uplink IQ sample width for UTRA FDD only	4	Logical connection
R-11A	Minimum uplink IQ sample width for WiMAX, E-UTRA, and GSM	8	Logical connection
R-12	Maximum uplink IQ sample width for UTRA FDD only	10	Logical connection
R-12A	Maximum uplink IQ sample width for WiMAX, E-UTRA, and GSM	20	Logical connection
R-13	Minimum downlink IQ sample width	8	Logical connection
R-14	Maximum downlink IQ sample width	20	Logical connection

Notes:

- Oversampling Factor of 2 or 4 is assumed for UTRA FDD in uplink
- Oversampling Factor of 1 or 2 is assumed for UTRA FDD in downlink
- Oversampling Factor of 1 is assumed for WiMAX and E-UTRA
- Oversampling Factor is not specified for GSM. The sampling rate may be:
    - either a multiple of the GSM symbol rates (1625/6 = 270.833kHz or 325kHz)
    - or a multiple or a sub-multiple of the UTRA FDD chip rate (3.84MHz)
- Automatic Gain Control may be used in uplink

[15] Former requirements R-5 ... R-9 have been merged to R-10. Requirement R-10 is not necessarily fulfilled by one link, but by the most efficient configuration (e.g. minimum number of links and most appropriate line rate) is preferable.

7.1.4.3. Required C&M-plane Bit Rate

The interface shall support a minimum bit rate for the M-plane transmission per link:

Requirement No.	Requirement Definition	Requirement Value	Scope
R-15	Minimum transmission rate of M-plane data (layer 1)	200 kbit/s	Link

Additionally, the interface shall support a minimum bit rate for the transmission of C-plane data per AxC:

Requirement No.	Requirement Definition	Requirement Value	Scope
R-16	Minimum transmission rate of C-plane data (layer 1)	25 kbit/s	Logical connection

The overhead on layer 2 due to frame delineation and frame check sequence depends on the frame length determined by higher layers. Assuming this overhead is well below 20%, a minimum net bit rate of 20kbit/s per AxC is available at the service access point SAP_{CM} as shown in Figure 2 and Figure 2A.

7.1.4.4. Required Real-Time Vendor Specific Bits

The interface shall provide additional bandwidth to transfer “Real-Time Vendor Specific Bits” in case of high line bit rates. The usage of “Real-Time Vendor Specific Bits” includes but is not limited to the following examples:

- To verify the quality of CPRI links by using CRC.
- To transfer auxiliary information for the IQ data, e.g. common exponents for multiple IQ samples in multiple AxC containers, and other auxiliary information used for IQ data compression.
- To transfer header information of vendor specific user plane data (which may not be IQ data) in multiple AxC containers.
- To extend U-plane IQ data transport.

Requirement No.	Requirement Definition	Requirement Value	Scope
R-16A	Minimum number of bits for Real-Time Vendor Specific Bits	32 bits per 1/3.84MHz	Link (line bit rate > 10.0Gbps)

7.1.5. Synchronization/Timing

7.1.5.1. Frequency Synchronization

The interface shall enable the RE to achieve the required frequency accuracy according to:

- 3GPP TS 25.104 [8] section 6.3 for UTRA FDD
- WiMAX Forum System Profile [11] section 4.2.4 for WiMAX
- 3GPP TS 36.104 [14], section 6.5.1 for E-UTRA
- 3GPP TS 45.010 [23], section 5.1 for GSM

The central clock for frequency generation in the RE shall be synchronized to the bit clock of one slave port. With 8B/10B or 64B/66B line coding the bit clock rate of the interface shall be a multiple of 3.84MHz in order to allow for a simple synchronization mechanism and frequency generation in the RE.

The impact of jitter on the frequency accuracy budget of the interface to the radio base station depends on the cut-off frequency of the RE synchronization mechanism. The interface shall accommodate a synchronization mechanism cut-off frequency high enough so that a standard crystal oscillator suffices as master clock of the RE. The contribution $\Delta f / f_0$ of the jitter τ to the frequency accuracy shall be defined with the cut-off frequency f_{CUT} as follows:

$$\frac{\Delta f}{f_0} = \frac{1}{f_0} \cdot \sqrt{\int_0^{f_{CUT}} f^2 \cdot 2 \cdot 10^{\frac{L(f)}{10dB}} \cdot df} \ , \quad (1)$$

where $L(f)$ is the single-side-band phase noise in dBc/Hz acquired on the interface with the following relation to the jitter τ :

$$\tau = \frac{1}{2 \cdot \pi \cdot f_0} \cdot \sqrt{\int_0^{f_0/2} 2 \cdot 10^{\frac{L(f)}{10dB}} \cdot df} \quad (2)$$

The reference point for the jitter and phase noise specification is a stable clock signal at the service access point SAP_S as shown in Figure 2. The frequency of this clock signal is denoted as f_0.

With f_{CUT} in equation (1) being the maximum allowed cut-off frequency, the impact of jitter on the radio base station frequency accuracy budget shall meet the following requirements:

Requirement No.	Requirement Definition	Requirement Value	Scope
R-17	Maximum allowed cut-off frequency f_{CUT} of RE synchronization	300 Hz	Link
R-18	Maximum contribution $\Delta f / f_0$ of jitter from the CPRI link to the radio base station frequency accuracy budget (between master SAP_S and slave SAP_S)	±0.002 ppm	Link

Any RE shall receive on its slave port a clock traceable to the main REC clock. This requires any RE reuses on its master ports a transmit clock traceable to REC, i.e. a clock retrieved from one of its slave ports.

Requirement No.	Requirement Definition	Requirement Value	Scope
R-18A	Receive clock on RE slave port	The clock shall be traceable to REC clock	Link

Traceable clock means the clock is produced from a “PLL” chain system with REC clock as input. “PLL” chain performance is out of CPRI scope.

7.1.5.2. Frame Timing Information

The synchronization part of the interface shall include mechanisms to provide precise frame timing information from the REC to the RE. The frame timing information shall be recovered on the RE in order to achieve the timing accuracy requirements as described in the sections below.

The RE shall forward frame timing information transparently when forwarding from a slave port to all the master ports. The frame timing information is allocated to the service access point SAP_S as shown in Figure 2. Timing accuracy and delay accuracy, as required in the subsections below, refer to the accuracy of timing signals at the service access point SAP_S. These timing signals shall be used in the RE for the precise timing of RF signal transmission and reception on the air interface.

7.1.5.3. Link Timing Accuracy

In this section the link accuracy requirement (R-19) is introduced based on the following requirements from the supported radio standards:

1. 3GPP UTRA-FDD Tx diversity and MIMO compliancy[16]
   The interface shall enable a radio base station to meet the requirement "time alignment error in Tx Diversity and MIMO transmission" (3GPP TS 25.104 [8] section 6.8.4).
2. 3GPP UTRA-FDD UE positioning with GPS timing alignment:
   The interface shall also support "UTRAN GPS Timing of Cell Frames for UE positioning" (3GPP TS 25.133 [9] section 9.2.10), which requires absolute delay accuracy.
3. WiMAX network synchronization with GPS (sections 8.3.7.1.1 and 8.4.10.1.1 of IEEE 802.16 [13])
4. E-UTRA Time alignment between transmitter branches
   The interface shall enable a radio base station to meet the requirement "time alignment between transmitter branches" (3GPP TS 36.104 [14], section 6.5.3).
5. GSM internal BTS carrier timing
   The timing difference between the different carriers shall be less than ¼ normal symbol periods, measured at the BTS antenna (3GPP TS 45.010 [23], section 5.3).

Requirement R-19 is based on the following three criteria:

a) Meet the 1st,4th and 5th requirement in a star configuration as shown in Figure 5:
   - for UTRA-FDD or E-UTRA, when TX diversity or MIMO signals belonging to one cell are transmitted via different REs;
   - for GSM, when different carriers are transmitted via different REs.

b) Meet the 2nd and 3rd requirement at any RE connected to the REC via multi-hop connection to the REC with the number of hops as given in R-4A.

c) Allow enough margin for additional delay tolerances in the RE implementation which is not part of CPRI.

The delay accuracy on one interface link excluding the group delay on the transmission medium, i.e. excluding the cable length, shall meet the following requirement.

Requirement No.	Requirement Definition	Requirement Value	Scope
R-19	Link delay accuracy in downlink between SAP_S master port and SAP_S slave port excluding the cable length.	$\pm$ 8.138ns [= $\pm T_C/32$]	Link

Note: The scope "link" for R-19 was chosen since the requirement R-19 can be met on a link. In multi-hop configurations the delay tolerances per link may add up, so the total tolerance may depend on the number of hops. Therefore it is not mandatory for CPRI to support a certain delay accuracy requirement for all multi-hop connections.

[16] With UTRA-FDD release 7, MIMO was introduced in the same section 6.8.4 of TS 25.104 [8] in addition to TX diversity without changing the specification value.

7.1.5.4. Round Trip Delay Accuracy

The round trip delay accuracy requirement (R-20) is introduced based on the following requirements from the supported radio standards:

- 3GPP UTRA-FDD, round trip time absolute accuracy
  The interface shall enable a radio base station to meet the requirement "round trip time absolute accuracy ±0.5 T_C" (3GPP TS 25.133 [9] section 9.2.8.1).
- 3GPP E-UTRA, timing advance
  The interface shall enable a radio base station to meet the Timing Advance report mapping minimum resolution of 65 ns (3GPP TS 36.133 [15], section 10.3).
- GSM, initial timing advance accuracy (3GPP TS 45.010 [23] section 5.4).
- GSM, delay tracking
  The interface shall enable a radio base station to meet the requirement "delay assessment error < ½ symbol period" (3GPP TS 45.010 [23] section 5.6).

The round trip time absolute accuracy of the interface, excluding the round trip group delay on the transmission medium (i.e., excluding the cable length), shall meet the following requirement.

Requirement No.	Requirement Definition	Requirement Value	Scope
R-20	Round trip absolute accuracy excluding cable length	± 16.276ns [= ±T_C/16]	Logical connection

Note: For round trip delay absolute accuracy even in multi-hop scenarios the delay tolerances per link do not add up as can be seen from the timing relations in section 4.2.9 and annex 6.1. Therefore the scope of requirement R-20 is "logical connection", which can be met in all configurations.

7.1.5.5. Accuracy of TDD Tx-Rx switching point

For WiMAX and E-UTRA TDD applications the Tx – Rx switching point needs to be transmitted per AxC. The required maximum contribution of the interface to the switching point accuracy shall meet the following requirement.

Requirement No.	Requirement Definition	Requirement Value	Scope
R-20A	Maximum contribution of the interface to the accuracy of TDD Tx-Rx switching point	± 16.276ns [= ±T_C/16]	Multi-hop connection

7.1.6. Delay Calibration

7.1.6.1. Round Trip Cable Delay per Link

The interface shall enable periodic measurement of the cable length of each link, i.e., measurement of the round trip group delay on the transmission medium of each link. The measurement results shall be available on the REC in order to meet the following requirements without the need to input the cable length to the REC by other means. The round trip delay accuracy requirement (R-21) is introduced based on the following requirements from the supported radio standards:

- "time alignment error in Tx Diversity shall not exceed ¼ T_C" (3GPP TS 25.104 [8] section 6.8.4)
- "round trip time absolute accuracy ±0.5 T_C" (3GPP TS 25.133 [9] section 9.2.8.1)

- "UTRAN GPS Timing of Cell Frames for UE positioning" (3GPP TS 25.133 [9] section 9.2.10)
- WiMAX network synchronization with GPS (sections 8.3.7.1.1 and 8.4.10.1.1 of IEEE 802.16 [13])
- E-UTRA, Timing Advance minimum resolution of 65 ns (3GPP TS 36.133 [15], section 10.3)
- GSM internal BTS carrier timing (3GPP TS 45.010 [23] section 5.3)
- GSM, initial timing advance accuracy (3GPP TS 45.010 [23] section 5.4)
- GSM, delay tracking (3GPP TS 45.010 [23] section 5.6)

The accuracy of the measurement of round trip group delay on the transmission medium of one link shall meet the following requirement:

Requirement No.	Requirement Definition	Requirement Value	Scope
R-21	Accuracy of the round trip delay measurement of cable delay of one link	± 16.276ns [= $\pm T_C/16$]	Link

7.1.6.2. Round Trip Delay of a Multi-hop Connection

The interface shall enable periodic measurement of the round trip group delay of each multi-hop connection. The measurement results shall be available on the REC in order to meet the following requirements without the need to input the cable lengths of the involved links to the REC by other means. The round trip delay accuracy requirement (R-21A) is introduced based on the following requirements from the supported radio standards:

- "round trip time absolute accuracy $\pm 0.5\ T_C$" (3GPP TS 25.133 [9] section 9.2.8.1)
- E-UTRA, Timing Advance minimum resolution of 65 ns (3GPP TS 36.133 [15] section 10.3)
- GSM, initial timing advance accuracy (3GPP TS 45.010 [23] section 5.4)
- GSM, delay tracking (3GPP TS 45.010 [23] section 5.6)

By measuring the round trip delay of the multi-hop connection directly, REC based computation of round trip delay shall be possible whatever the topology and the RE location within the branch, without adding delay tolerances of all links and networking REs used in the multi-hop connection.

The accuracy of the measurement of round trip group delay on the multi-hop connection shall meet the following requirement:

Requirement No.	Requirement Definition	Requirement Value	Scope
R-21A	Accuracy of the round trip delay measurement of the multi-hop connection	± 16.276ns [= $\pm T_C/16$]	Multi-hop connection

7.1.7. Link Maintenance

The layer 1 of the interface shall be able to detect and indicate loss of signal (LOS) and loss of frame (LOF) including frame synchronization. A remote alarm indication (RAI) shall be returned to the sender on layer 1 as a response to these errors. In addition the SAP defect indication (SDI) shall be sent to the remote end when any of the service access points is not valid due to an equipment error.

The signals

- LOS
- LOF
- SDI

- RAI

shall be handled within layer 1 and shall also be available to the higher layers of the interface.

Requirement No.	Requirement Definition	Requirement Value	Scope
R-22	Loss of Signal (LOS) detection and indication	-	Link
R-23	Loss of Frame (LOF) detection and indication	-	Link
R-24	SAP Defect Indication (SDI)	-	Link
R-25	Remote Alarm Indication (RAI)	-	Link

7.1.8. Quality of Service

7.1.8.1. Maximum Delay

In order to support efficient implementation of UTRA-FDD inner loop power control[17], the absolute round trip time for U-plane data (IQ data) on the interface, excluding the round trip group delay on the transmission medium (i.e. excluding the cable length), shall not exceed the following maximum value:

Requirement No.	Requirement Definition	Requirement Value	Scope
R-26	Maximum absolute round trip delay per link excluding cable length	5µs	Link

Round trip time is defined as the downlink delay plus the uplink delay. The delay is precisely defined as the time required transmitting a complete IQ sample over the interface. The availability and validity of an IQ sample is defined at the service access point SAP_{IQ} as shown in Figure 2. The precise point of time of availability and validity is indicated by the edge of an associated clock signal at the service access point SAP_{IQ} . The delay (e.g. in downlink) is defined as the time difference between the edge at the input SAP_{IQ} (e.g. on REC or RE) and the edge at the output SAP_{IQ} (e.g. on RE).

This definition is only valid for a regular transmission of IQ samples with a fixed sample clock.

7.1.8.2. Bit Error Ratio U-plane

The interface shall provide U-plane data transmission (on layer 1) with a maximum bit error ratio as specified below:

Requirement No.	Requirement Definition	Requirement Value	Scope
R-27	Maximum bit error ratio (BER) of U-plane	10^{-12}	Link

[17] Even with the introduction of new standards (e.g. WiMAX, E-UTRA, and GSM) UTRA FDD inner loop power control is still assumed to be the most time critical procedure constraining R-26

It should be a design goal to avoid forward error correction on layer 1 to achieve a cost efficient solution. There shall not be any data protection on layer 2.

7.1.8.3. Bit Error Ratio C&M-plane

The interface shall provide C&M-plane data transmission with a maximum bit error ratio (on layer 1) as specified below:

Requirement No.	Requirement Definition	Requirement Value	Scope
R-28	Maximum bit error ratio (BER) of C&M-plane	10^{-12}	Link

Additionally, a frame check sequence (FCS) shall be provided for C&M-plane data bit error detection on layer 2. The minimum length of the frame check sequence is defined in the following table:

Requirement No.	Requirement Definition	Requirement Value	Scope
R-29	Minimum length of frame check sequence (FCS)	16 bit	Link

7.1.8.4. CPRI Link Quality Monitoring

Layer 1 of the interface shall provide a mechanism for the higher layers to determine whether the link is operating within the CPRI specified limits as given in R-27 and R-28.

Requirement No.	Requirement Definition	Requirement Value	Scope
R-29A	Link quality monitoring	N/A	Link

7.1.9. Start-up Requirement

7.1.9.1. Clock Start-up Time Requirement

CPRI shall enable the RE clock to achieve synchronization with respect to the frequency accuracy and absolute frame timing accuracy within 10 seconds. The time needed for auto-negotiation of features (see Plug and Play requirement in section 7.1.9.2) is excluded from this requirement.

Requirement No.	Requirement Definition	Requirement Value	Scope
R-30	Maximum clock synchronization time	10 s	Link

7.1.9.2. Plug and Play Requirement

CPRI shall support auto-negotiation for selecting the line bit rate.

Requirement No.	Requirement Definition	Requirement Value	Scope
R-31	Auto-negotiation of line bit rate	-	Link
R-31A	Maximum number of line bit rate options on a master port for auto-negotiation.	At least 4	Link

CPRI shall support auto-negotiation for selecting the C&M-plane type and bit rate (layer 1).

Requirement No.	Requirement Definition	Requirement Value	Scope
R-32	Auto-negotiation of C&M-plane type and bit rate (layer 1)	-	Link

CPRI shall support auto-detection of REC data flow on slave ports:

Requirement No.	Requirement Definition	Requirement Value	Scope
R-33	Auto-detection of REC data flow on slave ports	-	Link

CPRI shall support auto-negotiation of scrambling:

Requirement No.	Requirement Definition	Requirement Value	Scope
R-34	Auto-negotiation of scrambling	-	Link

CPRI shall support auto-detection of the scrambling seed:

Requirement No.	Requirement Definition	Requirement Value	Scope
R-35	Auto-detection of scrambling seed	-	Link

8. List of Abbreviations

AC	Alternating Current
A/D	Analogue/Digital
ANSI	American National Standardization Institute
AxC	Antenna-carrier
BER	Bit Error Ratio
BFN	Node B Frame Number
C	Control
ceil()	The function “ceil” returns the smallest integer greater than or equal to the argument.
CP	Cyclic Prefix
C&M	Control and Management
CPRI	Common Public Radio Interface
D/A	Digital/Analogue
DA	Destination Address
DL	Downlink
EDGE	Enhanced Data Rates for GSM Evolution
ESD	End-of-Stream-Delimiter
E-UTRA	Evolved Universal Terrestrial Radio Access
f_C	Chip Rate of UTRA-FDD = 3.84MHz
FCS	Frame Check Sequence
FDD	Frequency Division Duplex
FFT	Fast Fourier Transform
floor()	The function “floor” returns the greatest integer less than or equal to the argument.
f_S	Sampling rate
GF	Galois Field
GPS	Global Positioning System
GSM	Global System for Mobile communications (Groupe Spécial Mobile)
HDLC	High-level Data Link Control
HFN	Hyper Frame Number
HV	High Voltage
I	In-Phase
IEC	International Electrotechnical Commission
IEEE	Institute of Electrical and Electronics Engineers
IFFT	Inverse Fast Fourier Transform
Iub	Interface between Radio Network Controller and UMTS radio base station (NodeB)
LCM	Least Common Multiple
LLC	Logical Link Control
Ln	Length
LOF	Loss of Frame

LOS	Loss of Signal
LSB	Least Significant Bit
LV	Low Voltage
LVDS	Low Voltage Differential Signal
M	Management
MAC	Media Access Control
MIMO	Multiple Input, Multiple Output
MSB	Most Significant Bit
N_{RB}	Number of resource blocks in an E-UTRA cell
N_{sc}^{RB}	Resource block size in the frequency domain, expressed as a number of subcarriers
N/A	Not Applicable
PAD	Padding
PCS	Physical Coding Sublayer
PDU	Protocol Data Unit
PHY	Physical Layer
PICS	Protocol Implementation Conformance Statement
PLL	Phase Locked Loop
PMA	Physical Medium Attachment
Q	Quadrature
QSFP	Quad Small Form-factor Pluggable
RAI	Remote Alarm Indication
RE	Radio Equipment
REC	Radio Equipment Control
RF	Radio Frequency
RRC	Root Raised Cosine
RTWP	Received Total Wideband Power
Rx	Receive
SA	Source Address
SAP	Service Access Point
SDI	SAP Defect Indication
SDU	Service Data Unit
SERDES	SerializerDeserializer
SFD	Start-of-Frame Delimiter
SFP	Small Form-factor Pluggable
SSD	Start-of-Stream Delimiter
T	Number of bits per word in a CPRI basic frame as defined in section 4.2.7.1
T_C	CPRI basic frame length = UTRA FDD Chip period = 1/3.84MHz
T_{CW}	Number of bits per control word in a CPRI basic frame as defined in section 4.2.7.1
T_F	WiMAX frame length
TP	Test Point

TS	Technical Specification
Tx	Transmit
UE	User Equipment
UL	Uplink
UTRA	Universal Terrestrial Radio Access (3GPP)
UTRAN	Universal Terrestrial Radio Access Network (3GPP)
UMTS	Universal Mobile Telecommunication System
Uu	UMTS air interface
WDM	Wavelength Division Multiplexing
WiMAX	Worldwide Interoperability for Microwave Access
XAUI	10 Gigabit Attachment Unit Interface
Z.X.W.Y	Byte Index (byte number Y, word number W, basic frame number X, hyperframe number Z)
#Z.X.W.Y	Content of byte with index Z.X.W.Y
Z.X.Y	Short form of BYTE Index, for **control BYTES only** (word number W = 0)
#Z.X.Y	Content of control BYTE with index Z.X.Y
3GPP	3rd Generation Partnership Project

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10. History

Version	Date	Description
V 1.0	2003-09-30	First complete CPRI specification
V 1.1	2004-05-10	• Editorial corrections. • Section 3: Clarification of input requirements for CPRI. • Section 4.2.7.5: An additional sequence K28.5 + D5.6 (defined in the 8B/10B standard as /I1/) is allowed for the use as control sync word to enable usage of existing SERDES devices. • Section 4.5.3.7: Editorial correction in subsection “RE actions” to align the text with Figure 30. • Section 5.1.4: Update of specification release version. • Section 5.2: Clarification of CPRI implementation compliancy.
V 1.2	2004-07-15	• Sections 4.2.2 to 4.2.4: Recommendation of a low voltage (CX based) and a high voltage (XAUI based) electrical interface. • Addition of Section 6.2. • Editorial changes and abbreviation addition.
V 1.3	2004-10-01	Major editorial correction in Section 4.5.4.4 and Section 4.5.4.12: • Exchange of BYTE index Z.64.0 with Z.66.0 • Exchange of BYTE index Z.192.0 with Z.194.0

V 2.0	2004-10-01	Introduction of the CPRI networking feature resulting in the following list of detailed modifications: Chapter 1: • Clarification of the CPRI scope (layers 1 + 2). • Clarification of the support mechanisms for redundancy. Section 2.1: • Additional definitions for node, link, passive link, hop, multi-hop, logical connection, master port and slave port. Section 2.2: • Update of system architecture introducing links between REs. Section 2.3: • Addition of chain, tree and ring topologies. Section 2.4: • Addition of the Section 2.4.2 on the CPRI control functionality. Chapter 3: • Adaptation of the requirements to the networking nomenclature. • Scope of each requirement has been added. Section 1: • Addition of chain, tree and ring topologies. • New requirements for no. of hops and ports have been added. Section 1: • Requirement of clock traceability for RE slave ports. Section 1: • Transparent forwarding of frame timing information. Section 3.5.3: • Renaming of section to link timing accuracy. • Clarification of requirement. Section 1: • Introduction of subsection 1 covering the round trip cable delay measurement requirements for the link. • Addition of subsection 1 on the round trip delay measurement requirements for a multi-hop connection. Section 1: • Requirement on the auto-detection of REC data flow on slave ports has been added.

		Section 4.2.7.6.1: • Forwarding of reset bit has been added. Section 4.2.7.6.2: • Clarification has been added that the filtering applies to reset as well as reset acknowledgement. Section 4.2.8: • Redefinition of synchronization and timing source. Section 4.2.9: • Renaming of section heading • Multi-hop case and multiple slave ports case are considered. • New reference points RB1-4 were defined. Figure 24A was added. • Timing relations of multi-hop configuration were defined. Figure 25A was added. Section 4.5: • REC is replaced by master port. • RE is replaced by slave port. • The terms “Uplink” and “Downlink” are replaced to avoid confusion in case of a ring topology. • The text of the sections defining transitions 1 and 11 is updated. Section 5.1.4: • Update of specification release version. Annex 6.1: • Delay calibration example for multi-hop configuration has been added. Annex 6.3: • Addition of an Annex called “Networking” aiming at giving examples of network capabilities of an REC and RE assumed in CPRI version 2.0. Section 7: • Update of list of abbreviations. Section 9: • Update of history. In addition, minor editorial corrections have been made.
V 2.1	2006-03-31	Chapters 3 and 8: • Update of the requirement no. R-1 as well as of References [8] and [9] to 3GPP UTRA FDD, Release 6, December 2005 Minor editorial correction in Section 4.2.7.5: • Table 9: Change X to 0: #Z.0.0 #Z.0.1 #Z.0.2 #Z.0.3

V 3.0	2006-10-20	Introduction of WiMAX resulting in the following list of detailed modifications: Chapter 2: • New definitions/nomenclature, system architecture, and functional split for WiMAX added Chapter 3: • Update of requirements R-1, R-5,…, R-12, R-19,…, R-21A, R-30 • New requirements for WiMAX: R-4F, R-11A, R-12A, R-20A Section 4.2.7.2: • WiMAX IQ mapping added including new subsections 4.2.7.2.4 through 4.2.7.2.7 • New subsection 4.2.7.2.8 for WiMAX TDD/FDD added Section 4.2.8 and section 6.1: • Synchronization and timing for WiMAX specified Section 5.1.4: • Protocol version number for CPRI V3.0 specified Introduction of line bit rate option 4 (3072.0Mbit/s) resulting in the following list of detailed modifications: Section 4.2.1: • New line bit rate option 4 listed Section 4.2.2: • Physical layer modes for line bit rate option 4 added Section 4.2.7.1: • Basic frame structure for line bit rate option 4 added Section 4.2.7.3: • Line bit rate option 4 added to hyperframe structure Section 4.2.7.5: • Synchronization control word for line bit rate option 4 specified Section 4.2.7.6 and section 4.2.7.7.1: • New configurations of slow C&M channel for line bit rate option 4 added Section 4.2.7.7.2: • New configurations of fast C&M channel for line bit rate option 4 added Section 6.2.: • Physical layer specification for line bit rate option 4 added Update of Chapters 7, 8, and 9. In addition, minor editorial corrections have been made.

V4.0	2008-06-30	Introduction of LTE & MIMO resulting in the following list of detailed modifications Chapter 2: • New definitions/nomenclature, system architecture, and functional split for E-UTRA added Chapter 3: • Update of requirements R-1, R-11A, R-12A, R-19, R-20, R-20A, R-21, R-21A, R-26 Section 4.2.7.2.: • E-UTRA IQ-mapping added Section 4.2.8 and section 6.1: • Synchronization and timing for E-UTRA specified • Figure 31 modified Section 5.1.4: • Protocol version number for CPRI V4.0 specified Chapter 6: • New informative section 6.4 “E-UTRA sampling rates” added Chapter 7: • Update of the abbreviation list Chapter 8: • Update of Reference list Introduction of multiple REC topologies resulting in the following list of detailed modifications: Chapter 1: • Scope of the specification modified in order to also cover multiple REC topologies Section 2.1: • Basic nomenclatures modified in order to also cover multiple REC topologies Section 2.3: • Multiple REC configurations added / new figures added showing multiple REC topologies Section 4.1, 4.2.9, 6.1: • Footnotes added Section 6.3: • New subsections 6.3.7 and 6.3.8 for multiple REC topologies added

		Addition of oversampling ratio 2 for UTRA FDD Downlink resulting in the following list of detailed modifications: Section 3.4.2: • Notes updated Section 4.2.7.2.2: • Modification of Table 5 and introduction of new Table 5A • Figure 11: figure caption modified In addition, the following modifications were done: Sections 3.5.3 and 3.5.4: • Addition of a note on the scope of TX delay being link (below R-19 and R-20 respectively) Section 3.5.3: • Improved wording of “Link Timing Accuracy" Section 4.2.2, 4.2.3, 4.2.4, 8 • Replacement of references to INCITS 352 by ISO/IEC 14165-115 Sections 4.2.2 – 4.2.5, 4.2.7.1.2, 4.4, 6.2, 8 • Replacement of references to IEEE 802.3 2002 / IEEE 802.3ae-2002 by IEEE Std 802.3-2005 Section 4.2.7.7.3: • Allowance of simple RE with no or simple C&M-link (use of non-zero C&M-channel is now recommended rather than mandatory) Section 4.5.3.2: • Slave port actions modified for improved LOS/LOF handling Section 9: • Update of history In addition, minor editorial corrections have been made.

V4.1	2009-02-18	Introduction of higher line bit rates (x8 and x10) for CPRI resulting in the following list of detailed modifications: a) Physical layer characteristics: Section 4.2.1: • New CPRI line bit rate options 5&6 introduced (8x & 10x) Section 4.2.2: • Table 2: New CPRI physical layer modes 4915.2 Mbps & 6144 Mbps included • Figure 6A: new LV-II variant included Sections 6.2, 6.2.1, 6.2.4, 6.2.6 and 6.2.7: • New LV-II variant adopted Sections 6.2.8.3 & 6.2.9.3 • New sections defining electrical Tx- & Rx-characteristics of LV-II Section 6.2.8.3: • Modified w.r.t. TX-compliance • LV-II variant included Section 6.2.9.4: • New section for Equalization and RX-compliance Section 4.2.2…4.2.4 & 8: • New reference [17] for OIF-CEI added • References to Fibre Channel Physical Interface-4, SFP and SFP+ introduced b) Introduction of data scrambling: Section 3.9.2: • New requirements R-34 and R-35 (Autonegotiation of Scrambling) Section 4.2.7.1.2: • New title: Transmission Sequence and Scrambling • Scrambling impact on transmission sequence defined Section 4.2.7.6: • New protocol version #Z.2.0 = 2 introduced in table 10 Section 4.2.10.3.1: • New Figure 26A (LOF and HFNSYNC detection with scrambling enabled)

		Section 5.1.4: • New specification release 4.1 added to table 15 • New protocol version number 2 introduced for this specification release in table 15 Section 6.5: • New normative scrambling section c) Impact on frame structure and HDLC-rate: Section 4.2.7: • Generic basic frame structure introduced (Figure 9B) • Table 6, 9 and 12 extended to also cover x8 & x10 line bit rates • Table 10 and 11 extended to also cover HDLC bit rate negotiation on higher layers • New Figure 22B Sections 4.5.3.4 & 4.5.3.5: • HDLC rate negotiation included In addition the following modifications were done: Sections 3.1 and 8 • New versions of the 3GPP and WiMAX Forum specifications adopted Section 3.5.3 • Time alignment between requirement between branches now defined in 3GPP TS 36.104 • Footnote eliminated Section 3.6.1 & 3.6.2: • Correction of delay calibration description Section 3.5.3 & 3.5.4: • Text improvements Section 4 & 6: • Consistent usage of Z.X.(W).Y and #Z.X.(W).Y

V4.2	2010-09-29	Introduction of higher line bit rate (16x) for CPRI resulting in the following list of detailed modifications: a) Physical layer characteristics: Section 4.2.1: • New CPRI line bit rate option 7 introduced (16x) Section 4.2.2: • Table 2: New CPRI physical layer mode 9830.4 Mbps included • Figure 6A: new LV-III variant included Section 4.2.2 & 8: • New reference [22] for IEEE Std 802.3™-2008 added Section 5.1.4: • New version 4.2 in Table 15 Sections 6.2, 6.2.1, 6.2.4, 6.2.6 and 6.2.7: • New LV-III variant adopted Sections 6.2.8.4 & 6.2.9.4 • New sections defining electrical Tx- & Rx-characteristics of LV-III Section 6.2.8.5 (former section 6.2.8.4): • LV-III variant included Section 6.2.9.5 (former section 6.2.9.4): • LV-III variant included Section 6.2.10: • New section “Low voltage III option” Section 6.5: • Table 21: new line bit rate 9830.4 Mbps b) Impact on frame structure and HDLC-rate: Section 4.2.7: • Table 3, 6, 9, 11 and 12 extended to also cover 16x line bit rate In addition the following modifications were done: Section 1 and cover page: • Removal of Nortel reference Sections 3.1, 3.5.4, 3.6.1, 3.6.2 and 8: • Update of 3GPP- and WiMAX-references • Removal of footnotes 3&4 Section 4.2.7.5: • Missing #Z.0.5 added to Table 9 Section 4.2.7.2.4 • Figure 13A corrected (s-3)

V5.0	2011-09-21	Introduction of GSM for CPRI resulting in the following list of detailed modifications: a) user plane data may not be IQ data: Section 2.1: • Update of user plane (data) definition • Update of AxC Container definition b) GSM specific references and requirements Sections 2, 2.2, 3.1, 3.4.2: • Inclusion of GSM as supported radio standard Section 3.5.1, 3.5.3, 3.5.4, 3.6: • GSM specific references & requirements added Section 8: • New references [23] & [24] added Section 7: • Add 'GSM' and 'EDGE' to the abbreviation list c) Functional decomposition for GSM added with Table 1AA in section 2.4.1 d) Introduction of GSM mantissa-exponent UL IQ format in sections 4.2.7.2.1 & 4.2.7.2.2 e) Introduction of GSM frame timing with new section 4.2.8.3 f) GSM mapping: Section 4.2.7.2.2: • AxC container usage in GSM case Section 4.2.7.2.7: • New Table 5D New informative section 6.6 (GSM sampling rates) g) Introduction of GSM associated AxC control: Section 2.1: • New definition: Ctrl_AxC Section 4.2.7.4: • Modification of Figure 15 and Table 7 New section 4.2.7.10: 'Control AxC Data' In addition the following modifications were done: in general spelling aligned: "synchronisation" → "synchronization" Section 5.1.4: update Table 15 Section 4.2.7.2.7: adopt WiMAX sample rate fs=22.4MHz to Table 5B Section 4.2.7.5: Table 9 corrected to 5 control Bytes for 3072Mbit/s Section 4.5.2: Figure 30 corrected ("missmatch" → "mismatch") Section 6.2.9.2: Table number "Table 20" corrected to "Table 19Z Section 9, history of V4.1: Requirement numbers for scrambling corrected to R-34 & R-35

V6.0	2013-08-30	Introduction of LTE-Advanced for CPRI resulting in the following list of detailed modifications: Section 3.1: update 3GPP E-UTRA, release to 10, March 2012 Section 3.4.1: • add component carrier definition and capacity values • remove R5..R9 and have more generic R10 instead Section 6.4: • update reference table number in 3GPPTS36.104 • introduce lower sample rate options for LTE15 & 20 in Table 20 Introduction of new Basic Frame structure (T_{CW}=128) resulting in the following list of detailed modifications: Section 4.2.7.1.1: introduction of T_{CW} (also in Table 3) Section 4.2.7.1.2: new figure 9C: generic frame structure with $T_{CW} \neq T$ Section 4.2.7.3: update Table 6 with new line bit rate Section 4.2.7.7.1: update Table 11 with new line rate / replace T by T_{CW} Section 4.2.7.7.2: update Table 12 with new line bit rate Section 4.2.7.10: replace T by T_{CW} (also in figure 23Z) Introduction of 64B/66B line coding resulting in the following list of changes: Section 3.5.1: 64B/66B added Section 4.2.1: CPRI line bit rate option 8 added Section 4.2.2: 10137.6 Mbps added to Table 2 & Figure 6A updated Section 4.2.5: new 64B/66B line coding scheme added Section 4.2.6: detection of sync header violations in 64B/66B case Section 4.2.7.1.2: distinction between 8B/10B and 64B/66B Section 4.2.7.4: Fig. 15 updated (Z.0.0) / reference to new table 9A Section 4.2.7.5: Table 8: Z.0.0 specific line updated, new Table 9A Section 4.2.8: CPRI 10ms frame delimiter Z.0.0 instead of K28.5 Section 4.2.10.2.1: New LOS detection criterion for 64B/66B line coding Section 4.2.10.2.2: New LOS cease criterion for 64B/66B line coding Section 4.2.10.3.1: new figure 26B Section 4.5.3.2/4.5.3.3: interpreted control bytes line coding specific Section 5.1.1: Sync and Timing control byte line coding specific Section 5.1.4: 64B/66B and new release version adopted to Table 15 Section 6.5: Scope limited to 8B10B line coding Section 6.7: New Introduction of CPRI link quality monitoring resulting in following changes: Section 3.8.4 CPRI Link Quality Monitoring: New Section 4.2.10.6 Link quality monitoring: New Additions to line bit rate autonegotion resulting in following changes: Section 3.9.2: new req. R-31A Section 4.5.3.2: highlighted, that hanging-up might also occur if master port support more then 4 line bit rates Section 6.8: New informative section In addition the following modifications were done: Section 3.4.4: New (Required Real-Time Vendor Specific bits) Section 4.2.10.3.1: Figure 26A updated (brackets updated) Section 8: References updated; new reference [25]

V6.1	2014-07-01	Editorial clean-up: • Section 4.2.7.1.2: Figure 9B and 9C moved to 9A and 9B • Section 4.2.7.7.1: Figure 22B moved to 22, figure 22 and 22A removed • Replacement of references to IEEE 802.3-2005 by IEEE Std 802.3-2012 • Company name changed from Nokia Siemens Networks to Nokia Networks Introduction of new CPRI line bit rates: • 8110.08Mbps (64/66B coding) and • 12165.12Mbps (64B/66B coding) • Section 4.2.1: option 7A and option 9 added • Section 4.2.2: update of Table 2, footnote, Figure 6A • Section 4.2.2: reference to Fiber Channel (FC-PI-5) standard added • Section 4.2.2: recommendation for reuse of SERDES components removed • Section 4.2.5: option 7A and 9 added • Section 4.2.7: update of Table 3, Table 6, Table 9A, Table 11 and Table 12 • Section 6.2.1: update of Figure 32 • Section 6.2.8: update of Table 18B • Section 6.2.9: update of Table 19A/19B • Section 6.2.8.4: Figure 37B corrected • Section 7.1.5.1: line bit rate shall be a multiple of 3.84MHz • Section 9: reference [28] added Support of Wavelength Division Multiplexing (WDM) and QSFP+ optical transceiver added • Section 4.2.2: updated • Section 4.2.4: reference to QSFP+ standard added • Section 9: references [26], [27] added Section 3. moved to section 7.1 of Annex B Reference to Protocol Implementation Conformance Statement (PICS) added • Section 5.2 GSM case added in stuffing bit definition (Section 2.1)