JESD204B Survival Guide

Practical JESD204B Technical Information, Tips, and Advice from the World's Data Converter Market Share Leader*

*Analog Devices has a 48.5% global data converter market share, which is more than the next eight competitors combined, according to the analyst firm Databeans in its 2011 Data Converters Report.

www.analog.com

ANALOG DEVICES

Contents

What Is JESD204 and Why Should We Pay Attention to It?

by Jonathan Harris, Applications Engineer, Analog Devices, Inc.

A new converter interface is steadily picking up steam and looks to become the protocol of choice for future converters. This new interface, JESD204, was originally rolled out several years ago but has undergone revisions that are making it a much more attractive and efficient converter interface. As the resolution and speed of converters has increased, the demand for a more efficient interface has grown. The JESD204 interface brings this efficiency and offers several advantages over its CMOS and LVDS predecessors in terms of speed, size, and cost. Designs employing JESD204 enjoy the benefits of a faster interface to keep pace with the faster sampling rates of converters. In addition, there is a reduction in pin count which leads to smaller package sizes and a lower number of trace routes that make board designs much easier and offers lower overall system cost. The standard is also easily scalable so it can be adapted to meet future needs. This has already been exhibited by the two revisions that the standard has undergone. The JESD204 standard has seen two revisions since its introduction in 2006 and is now at Revision B. As the standard has been adopted by an increasing number of converter vendors and users, as well as FPGA manufacturers, it has been refined and new features have been added that have increased efficiency and ease of implementation. The standard applies to both analog-to-digital converters (ADCs), as well as digital-to-analog converters (DACs) and is primarily intended as a common interface to FPGAs (but may also be used with ASICs).

JESD204—WHAT IS IT?

In April of 2006, the original version of JESD204 was released. The standard describes a multigigabit serial data link between converter(s) and a receiver, commonly a device such as an FPGA or ASIC. In this original version of JESD204, the serial data link was defined for a single serial lane between a converter or multiple converters and a receiver. A graphical representation is provided in Figure 1. The lane shown is the physical interface between M number of converters and the receiver which consists of a differential pair of interconnect utilizing current mode logic (CML) drivers and receivers. The link shown is the serialized data link that is established between the converter(s) and the receiver. The frame clock is routed to both the converter(s) and the receiver and provides the clock for the JESD204 link between the devices.

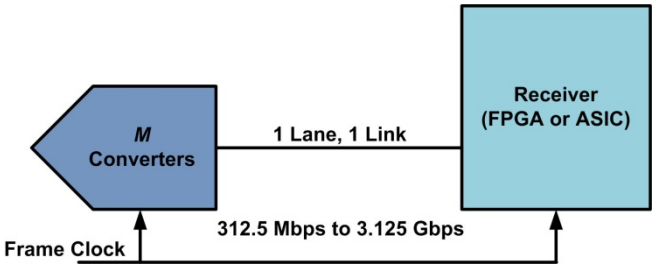


Figure 1. JESD204 Original Standard

The lane data rate is defined between 312.5 Megabits per second (Mbps) and 3.125 Gigabits per second (Gbps) with both source and load impedance defined as 100 Ω ±20%. The differential voltage level is defined as being nominally 800 mV peak-to-peak with a common-mode voltage level range from 0.72 V to 1.23 V. The link utilizes 8b/10b encoding which incorporates an embedded clock, removing the necessity for routing an additional clock line and the associated complexity of aligning an additional clock signal with the transmitted data a high data rates. It became obvious, as the JESD204 standard began gaining popularity, that the standard needed to be revised to incorporate support for multiple aligned serial lanes with multiple converters to accommodate increasing speeds and resolutions of converters.

This realization led to the first revision of the JESD204 standard in April of 2008 which became known as JESD204A. This revision of the standard added the ability to support multiple aligned serial lanes with multiple converters. The lane data rates, supporting from 312.5 Mbps up to 3.125 Gbps, remained unchanged as did the frame clock and the electrical interface specifications. Increasing the capabilities of the standard to support multiple aligned serial lanes made it possible for converters with high sample rates and high resolutions to meet the maximum supported data rate of 3.125 Gbps. Figure 2 shows a graphical representation of the additional capabilities added in the JESD204A revision to support multiple lanes.

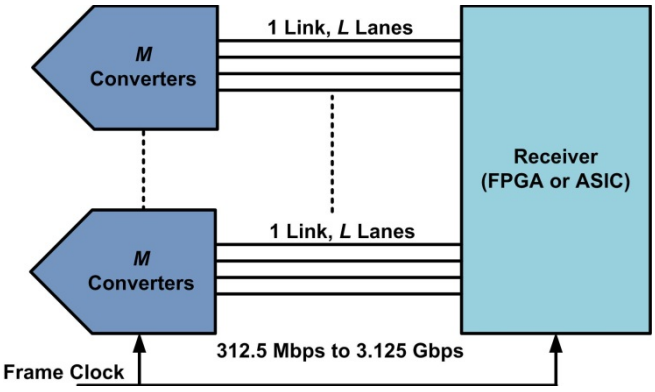


Figure 2. First Revision—JESD204A

Although both the original JESD204 standard and the revised JESD204A standard were higher performance than legacy interfaces, they were still lacking a key element. This missing element was deterministic latency in the serialized data on the link. When dealing with a converter, it is important to know the timing relationship between the sampled signal and its digital representation in order to properly recreate the sampled signal in the analog domain once the signal has been received (this situation is, of course, for an ADC, a similar situation is true for a DAC). This timing relationship is affected by the latency of the converter which is defined for an ADC as the number of clock cycles between the instant of the sampling edge of the input signal until the time that its digital representation is present at the converter's outputs. Similarly, in a DAC, the latency is defined as the number of clock cycles between the time the digital signal is clocked into the DAC until the analog output begins changing. In the JESD204 and JESD204A standards, there were no defined capabilities that would deterministically set the latency of the converter and its serialized digital inputs/outputs. In addition, converters were continuing to increase in both speed and resolution. These factors led to the introduction of the second revision of the standard, JESD204B.

In July of 2011, the second and current revision of the standard, JESD204B, was released. One of the key components of the revised standard was the addition of provisions to achieve deterministic latency. In addition, the data rates supported were pushed up to 12.5 Gbps, broken down into different speed grades of devices. This revision of the standard calls for the transition from using the frame clock as the main clock source to using the device clock as the main clock source. Figure 3 gives a representation of the additional capabilities added by the JESD204B revision.

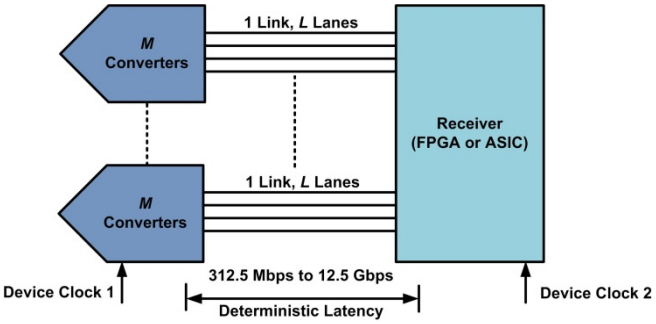


Figure 3. Second (Current) Revision—JESD204B

In the previous two versions of the JESD204 standard, there were no provisions defined to ensure deterministic latency through the interface. The JESD204B revision remedies this issue by providing a mechanism to ensure that, from power-up cycle to power-up cycle and across link re-synchronization events, the latency should be repeatable and deterministic. One way this is accomplished is by initiating the initial lane alignment sequence in the converter(s) simultaneously across all lanes at a well-defined moment in time by using an input signal called SYNC~. Another implementation is to use the SYSREF signal which is a newly defined signal for JESD204B. The SYSREF signal acts as the master timing reference and aligns all the internal dividers from device clocks as well as the local multiframe clocks in each transmitter and receiver. This helps to ensure deterministic latency through the system. The JESD204B specification calls out three device subclasses: Subclass 0—no support for deterministic latency, Subclass 1—deterministic latency using SYSREF, and Subclass 2—deterministic latency using SYNC~. Subclass 0 can simply be compared to a JESD204A link. Subclass 1 is primarily intended for converters operating at or above 500 MSPS while Subclass 2 is primarily for converters operating below 500 MSPS.

In addition to the deterministic latency, the JESD204B version increases the supported lane data rates to 12.5 Gbps and divides devices into three different speed grades. The source and load impedance is the same for all three speed grades being defined as 100 Ω ±20%. The first speed grade aligns with the lane data rates from the JESD204 and JESD204A versions of the standard and defines the electrical interface for lane data rates up to 3.125 Gbps. The second speed grade in JESD204B defines the electrical interface for lane data rates up to 6.375 Gbps. This speed grade lowers the minimum differential voltage level to 400 mV peak-to-peak, down from 500 mV peak-to-peak for the first speed grade. The third speed grade in JESD204B defines the electrical interface for lane data rates up to 12.5 Gbps. This speed grade lowers the minimum differential voltage level required for the electrical interface to 360 mV peak-to-peak. As the lane data rates increase for the speed grades, the minimum required

differential voltage level is reduced to make physical implementation easier by reducing required slew rates in the drivers.

To allow for more flexibility, the JESD204B revision transitions from the frame clock to the device clock. Previously, in the JESD204 and JESD204A revisions, the frame clock was the absolute timing reference in the JESD204 system. Typically, the frame clock and the sampling clock of the converter(s) were usually the same. This did not offer a lot of flexibility and could cause undesired complexity in system design when attempting to route this same signal to multiple devices and account for any skew between the different routing paths. In JESD204B, the device clock is the timing reference for each element in the JESD204 system. Each converter and receiver receives their respective device clock from a clock generator circuit which is responsible for generating all device clocks from a common source. This allows for more flexibility in the system design but requires that the relationship between the frame clock and device clock be specified for a given device.

JESD204—WHY SHOULD WE PAY ATTENTION TO IT?

In much the same way as LVDS began overtaking CMOS as the technology of choice for the converter digital interface several years ago, JESD204 is poised to tread a similar path in the next few years. While CMOS technology is still hanging around today, it has mostly been overtaken by LVDS. The speed and resolution of converters as well as the desire for lower power eventually renders CMOS and LVDS inadequate for converters. As the data rate increases on the CMOS outputs, the transient currents also increase and result in higher power consumption. While the current, and thus, power consumption, remains relatively flat for LVDS, the interface has an upper speed bound that it can support. This is due to the driver architecture, as well as the numerous data lines that must all be synchronized to a data clock. Figure 4 illustrates the different power consumption requirements of CMOS, LVDS, and CML outputs for a dual 14-bit ADC.

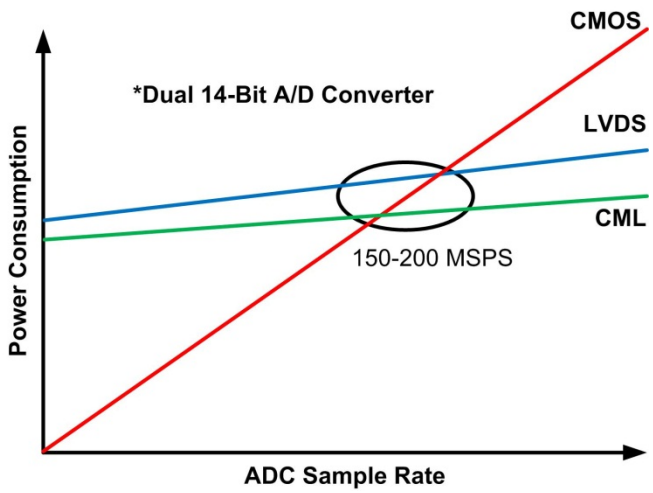


Figure 4. CMOS, LVDS, and CML Driver Power Comparison

At approximately 150 MSPS to 200 MSPS and 14 bits of resolution, CML output drivers start to become more efficient in terms of power consumption. CML offers the advantage of requiring less number of output pairs per a given resolution than LVDS and CMOS drivers due to the serialization of the data. The CML drivers specified for the JESD204B interface have an additional advantage since the specification calls for reduced peak-to-peak voltage levels as the sample rate increases and pushes up the output line rate. The number of pins required for the same give converter resolution and sample rate is also considerably less. Table 1 gives an illustration of the pin counts for the three different interfaces using a 200 MSPS converter with various channel counts and bit resolutions. The data assumes a synchronization clock for each channel's data in the case of the CMOS and LVDS outputs and a maximum data rate of 4.0 Gbps for JESD204B data transfer using the CML outputs. The reasons for the progression to JESD204B using CML drivers become obvious when looking at this table and observing the dramatic reduction in pin count that can be achieved.

Table 1. Pin Count Comparison—200 MSPS ADC

Number of Channels	Resolution	CMOS Pin Count	LVDS Pin Count (DDR)	CML Pin Count (JESD204B)
1	12	13	14	2
2	12	26	28	4
4	12	52	56	8
8	12	104	112	16
1	14	15	16	2
2	14	30	32	4
4	14	60	64	8
8	14	120	128	16
1	16	17	18	2
2	16	34	36	4
4	16	68	72	8
8	16	136	144	16

Analog Devices, Inc., market leader in data converters, has seen the trend that is pushing the converter digital interface towards the JESD204 interface defined by JEDEC. Analog Devices has been involved with the standard from the beginning when the first JESD204 specification was released. To date, Analog Devices has released to production several converters with the JESD204 and JESD204A compatible outputs and is currently developing products with outputs that are compatible with JESD204B. The AD9639 is a quad-channel 12-bit 170 MSPS/210 MSPS ADC that has a JESD204 interface. The AD9644 and AD9641 are 14-bit 80 MSPS/155 MSPS dual and single ADCs that have the JESD204A interface. From the DAC perspective, the recently released AD9128 is a dual 16-bit 1.25 GSPS DAC that has a JESD204A interface. For more information on Analog Devices efforts in regards to JESD204, please visit www.analog.com/jesd204.

As the speed and resolution of converters have increased, the demand for a more efficient digital interface has increased. The industry began realizing this with the JESD204 serialized data interface. The interface specification has continued to evolve to offer a better and faster way to transmit data between converters and FPGAs (or ASICs). The interface has undergone two revisions to improve upon its implementation and meet the increasing demands brought on by higher speeds and higher resolution converters. Looking to the future of converter digital interfaces, it is clear that JESD204 is poised to become the industry choice for the digital interface to converters. Each revision has answered the demands for improvements on its implementation and has allowed the standard to evolve to meet new requirements brought on by changes in converter technology. As system designs become more complex and converter performance pushes higher, the JESD204 standard should be able to adapt and evolve to continue to meet the new design requirements necessary.

REFERENCES

JEDEC Standard JESD204 (April 2006). JEDEC Solid State Technology Association. www.jedec.org.

JEDEC Standard JESD204A (April 2008). JEDEC Solid State Technology Association. www.jedec.org.

JEDEC Standard JESD204B (July 2011). JEDEC Solid State Technology Association. www.jedec.org.

RESOURCES

Share this article on

ABOUT THE AUTHOR

Jonathan Harris is a product applications engineer in the High Speed Converter Group at Analog Devices (Greensboro, NC). He has over seven years of experience as an applications engineer, supporting products in the RF industry. Jonathan received his MSEE from Auburn University and his BSEE from UNC-Charlotte. He can be reached via email at jonathan.harris@analog.com.

One Technology Way • P.O. Box 9106 • Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 • Fax: 781.461.3113 • www.analog.com
Trademarks and registered trademarks are the property of their respective owners.
TA11322-0-10/13(A)

High Speed Converter Survival Guide: Digital Data Outputs

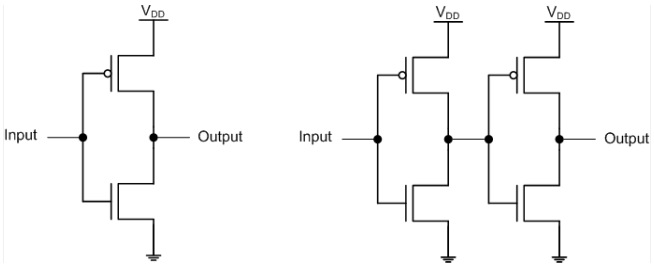
by Jonathan Harris, Product Applications Engineer, Analog Devices, Inc.

IDEA IN BRIEF

With a multitude of analog-to-digital converters (ADCs) available for designers to choose from, an important parameter to consider in the selection process is the type of digital data outputs included. Currently, the three most common types of digital outputs utilized by high speed converters are complementary metal oxide semiconductor (CMOS), low voltage differential signaling (LVDS), and current mode logic (CML). Each of these digital output types used in ADCs has its advantages and disadvantages that designers should consider in their particular application. These factors depend on the sampling rate and resolution of the ADC, the output data rates, the power requirements of the system design, and others. In this article, the electrical specifications of each type of output will be discussed along with what makes each type suited for its particular application. These different types of outputs will be compared in terms of physical implementation, efficiency, and the applications best suited for each type.

CMOS DIGITAL OUTPUT DRIVERS

In ADCs with sample rates of less than 200 MSPS, it is common to find that the digital outputs are CMOS. A typical CMOS driver employed consists of two transistors, one NMOS and one PMOS, connected between the power supply (V_{DD}) and ground, as shown in Figure 1a. This structure results in an inversion in the output, so as an alternative, the back-to-back structure in Figure 1b can be used in order to avoid the inversion in the output. The input of the CMOS output driver is high impedance while the output is low impedance. At the input to the driver, the impedance of the gates of the two CMOS transistors is quite high since the gate is isolated from any conducting material by the gate oxide. The impedances at the input can range from kilo ohms to mega ohms. At the output of the driver, the impedance is governed by the drain current, I_D, which is typically small. In this case, the impedance is usually less than a few hundred ohms. The voltage levels for CMOS swing from approximately V_{DD} to ground and can, therefore, be quite large depending on the magnitude of V_{DD}.



a) Inverted Output b) Noninverted Output

Figure 1. Typical CMOS Digital Output Driver

Since the input impedance is high and the output impedance is relatively low, an advantage that CMOS has is that one output can typically drive multiple CMOS inputs. Another advantage to CMOS is the low static current. The only instance where there is significant current flow is during a switching event on the CMOS driver. When the driver is in either a low state, pulled to ground, or in a high state, pulled to V_{DD}, there is little current flow through the driver. However, when the driver is switching from a low state to a high state or from a high state to a low state, there is a momentary low resistance path from V_{DD} to ground. This transient current is one of the main reasons why other technologies are used for output drivers when converter speeds go beyond 200 MSPS.

Another reason to note is that a CMOS driver is required for each bit of the converter. If a converter has 14 bits, there are 14 CMOS output drivers required to transmit each of those bits. Commonly, more than one converter is placed in a given package, and up to eight converters in a single package are common. When using CMOS technology, this could mean that there would be up to 112 output pins required just for the data outputs. Not only would this be inhibitive from a packaging standpoint, but it would also have high power consumption and increase the complexity of board layout. To combat these issues, an interface using low voltage differential signaling (LVDS) was introduced.

LVDS DIGITAL OUTPUT DRIVERS

LVDS offers some nice advantages over CMOS technology. It operates with a low voltage signal, approximately 350 mV, and is differential rather than single ended. The lower voltage swing has a faster switching time and reduces EMI concerns. By virtue of being differential, there is also the benefit of

common-mode rejection. This means that noise coupled to the signals tends to be common to both signal paths and is mostly cancelled out by the differential receiver. The impedances in LVDS need to be more tightly controlled. In LVDS, the load resistance needs to be approximately 100 Ω and is usually achieved by a parallel termination resistor at the LVDS receiver. In addition, the LVDS signals need to be routed using controlled impedance transmission lines. The single-ended impedance required is 50 Ω while the differential impedance is maintained at 100 Ω. Figure 2 shows the typical LVDS output driver.

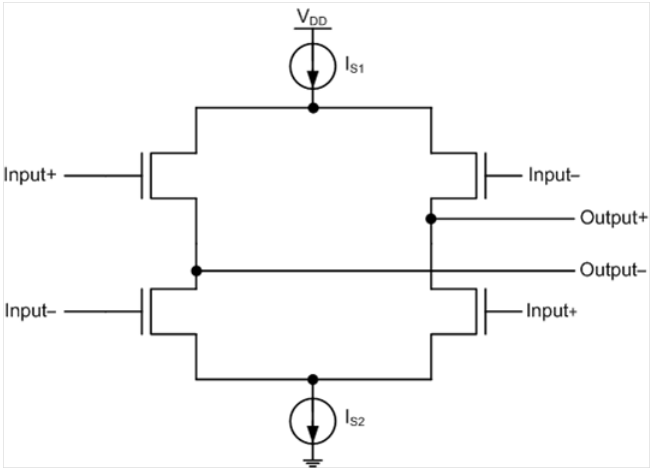


Figure 2. Typical LVDS Output Driver

As can be seen by the topology of the LVDS output driver in Figure 2, the circuit operation results in a fixed dc load current on the output supplies. This avoids current spikes that would be seen in a typical CMOS output driver when the output logic state transitions. The nominal current source/sink in the circuit is set to 3.5 mA which results in a typical output voltage swing of 350 mV with a 100 Ω termination resistor. The common-mode level of the circuit is typically set to 1.2 V, which is compatible with 3.3 V, 2.5 V, and 1.8 V supply voltages.

There are two standards that have been written to define the LVDS interface. The most commonly used is the ANSI/TIA/EIA-644 specification entitled "Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits." The other is the IEEE standard 1596.3 entitled "IEEE Standard for Low Voltage Differential Signals (LVDS) for Scalable Coherent Interface (SCI)."

LVDS does require that special attention be paid to the physical layout of the routing of the signals but offers many advantages for converters when sampling at speeds of 200 MSPS or greater. The constant current of the LVDS driver allows for many outputs to be driven without the large amount of current draw that CMOS would require. In addition, it is possible to operate LVDS in a double-data rate (DDR) mode where two data bits can be routed through the same LVDS output driver. This reduces the number of pins required by one half compared to CMOS. In addition, the amount of power consumed for the same number of data outputs is reduced. LVDS does offer numerous benefits over CMOS for the data outputs of converters, but it eventually has its limitations as CMOS does. As converter resolution increases, the number of data outputs required by an LVDS interface becomes more difficult to manage for PCB layouts. In addition, the sample rates of converters eventually push the required data rates of the interface beyond the capabilities of LVDS.

CML OUTPUT DRIVERS

The latest trend in digital output interfaces for converters is to use a serialized interface that uses current mode logic (CML) output drivers. Typically, converters with higher resolutions (≥14 bits), higher speeds (≥200 MSPS), and the desire for smaller packages with less power utilize these types of drivers. The CML output driver is employed in JESD204 interfaces that are being used on the latest converters.

Utilizing CML drivers with serialized JESD204 interfaces allows data rates on the converter outputs to go up to 12 Gbps (with the current revision of the specification JESD204B). In addition, the number of output pins required is dramatically reduced. Routing a separate clock signal is no longer necessary since the clock becomes embedded in the 8b/10b encoded data stream. The number of data output pins is also reduced with a minimum of two being required. As the resolution, speed, and channel count of the converter increase, the number of data output pins may be scaled to account for the greater amount of throughput required. Since the interface employed with CML drivers is typically serial, however, the increase in the number of pins required is much smaller than that compared with CMOS or LVDS (the data transmitted in CMOS or LVDS is parallel, which requires a much great number of pins).

Since CML drivers are employed in serialized data interfaces, the number of pins required is much smaller. Figure 3 shows a typical CML driver used for converters with JESD204 or similar data outputs. The figure gives a generalization of the typical architecture of a CML driver. It shows the optional source termination resistor and the common-mode voltage. The inputs to the circuit drive the switches to the current sources which drive the appropriate logic value to the two output terminals.

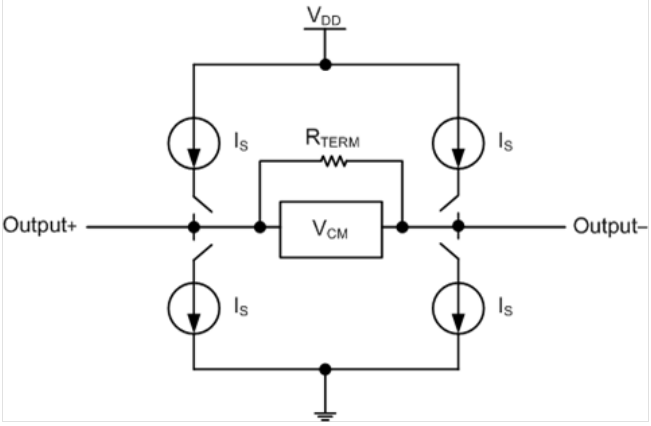


Figure 3. Typical CML Output Driver

A CML driver is similar to the LVDS driver in that it operates in a constant current mode. This also gives the CML driver an advantage in terms of power consumption. Operating in a constant current mode requires fewer output pins, and the total power consumption is reduced. As with LVDS, a load termination is required, as well as controlled impedance transmission lines having a single-ended impedance of 50 Ω and a differential impedance of 100 Ω. The driver itself may also have terminations, as shown in Figure 3, to help with any signal reflections due to the sensitivity with such high bandwidth signals. In converters employing the JESD204 standard, there are different specifications for the differential and common-mode voltage levels depending upon the speed of operation. Operating at speeds up to 6.375 Gbps, the differential voltage level is nominally 800 mV while the common mode is approximately 1.0 V. When operating above speeds of 6.375 Gbps, but less than 12.5 Gbps, the differential voltage level is specified at 400 mV while the common mode is again approximately 1.0 V. As converter speed and resolution increase, CML outputs look to be the desired driver type to deliver the speeds necessary to keep pace with technology demands placed on converters for their various applications.

DIGITAL TIMING—THINGS TO LOOK OUT FOR

Each of the digital output driver types has timing relationships that need to be monitored closely. Since there are multiple data outputs with CMOS and LVDS, attention must be directed to the routing paths of the signals to minimize skew. If there is too large of a difference, then proper timing at the receiver may not be achieved. In addition, there is a clock signal that needs to be routed and aligned with the data outputs. Careful attention must be given to the routing paths between the clock output, and also the data outputs, to ensure that the skew is not too large.

In the case of CML in the JESD204 interface, attention must also be directed to the routing paths between the digital outputs. There are significantly less data outputs to manage, so this task does become easier but cannot be neglected altogether. In this case, there should be no concern with regards to timing skew between the data outputs and the clock output since the clock is embedded in the data. However, attention must be given to an adequate clock and data recovery (CDR) circuit in the receiver.

In addition to the skew, the setup and hold times must also be given attention with CMOS and LVDS. The data outputs must be driven to their appropriate logic state in sufficient time before the edge transition of the clock and must be maintained in that logic state for a sufficient time after the edge transition of the clock. This can be affected by the skew between the data outputs and the clock outputs, so it is important to maintain good timing relationships. LVDS has the advantage over CMOS due to the lower signal swings and differential signaling. The LVDS output driver does not have to drive such a large signal to many different outputs and does not draw a large amount of current from the power supply when switching logic states, as the CMOS driver would. This makes it less likely for there to be an issue delivering a change in logic state. If there were many CMOS drivers switching simultaneously, the power supply voltage could get pulled down and introduce issues driving the right logic values to the receiver. The LVDS drivers would maintain a constant level of current such that this particular issue would not arise. In addition, the LVDS drivers are inherently more immune to common-mode noise due to its use of differential signaling. The CML drivers have similar benefits to LVDS. These drivers also have a constant level of current, but unlike LVDS, fewer numbers are required due to the serialization of the data. In addition, the CML drivers also offer immunity to common-mode noise since they also use differential signaling.

As converter technology has progressed with increased speeds and resolutions, the digital output drivers have adapted and evolved to meet the requirements necessary to transmit data. CML outputs are becoming more popular as the digital output interfaces in converters transition to serialized data transmission. However, CMOS and LVDS digital outputs are still being utilized today in current designs. There are applications where each type of digital output is best suited and makes the most sense to use. Each type of output comes with challenges and design considerations, and each type of output has its advantages. In converters with sampling speeds less than 200 MSPS, CMOS is still an appropriate technology to employ. When sampling speeds increase above 200 MSPS, LVDS becomes a more viable option in many applications as compared to CMOS. To further increase

efficiency and reduce power and package size, CML drivers can be employed with a serialized data interface such as JESD204.

REFERENCES

Bloomingdale, Cindy and Gary Hendrickson. AN-586 Application Note. *LVDS Data Outputs for High-Speed Analog-to-Digital Converters.* Analog Devices, Inc., 2002.

JEDEC Standard JESD204 (April 2006). JEDEC Solid State Technology Association. www.jedec.org.

JEDEC Standard JESD204A (April 2008). JEDEC Solid State Technology Association. www.jedec.org.

JEDEC Standard JESD204B (July 2011). JEDEC Solid State Technology Association. www.jedec.org.

ABOUT THE AUTHOR

Jonathan Harris is a product applications engineer in the High Speed Converter Group at Analog Devices (Greensboro, NC). He has over seven years of experience as an applications engineer, supporting products in the RF industry. Jonathan received his MSEE from Auburn University and his BSEE from UNC-Charlotte. He can be reached via email at jonathan.harris@analog.com.

RESOURCES

Share this article on

One Technology Way • P.O. Box 9106 • Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 • Fax: 781.461.3113 • www.analog.com
Trademarks and registered trademarks are the property of their respective owners. TA11328-0-1/13

JESD204B vs. Serial LVDS Interface Considerations for Wideband Data Converter Applications

by George Diniz, Product Line Manager, Analog Devices, Inc.

IDEA IN BRIEF

The JESD204A/JESD204B industry standard for serial interfaces was developed to address the problem of interconnecting the newest wideband data converters with other system ICs in an efficient and cost saving manner. The motivation was to standardize an interface that would reduce the number of digital inputs/outputs between data converters and other devices, such as FPGAs (field programmable gate arrays) and SoCs (systems on a chip), through the use of a scalable high speed serial interface.

Trends show that new applications, as well as advances in existing ones, are driving the need for wideband data converters with increasingly higher sampling frequencies and data resolutions. Transmitting data to and from these wideband converters poses a significant design problem as bandwidth limitations of existing I/O technologies force the need for higher pin counts on converter products. Consequently, systems PCB designs have become increasingly more complex in terms of interconnect density. The challenge is routing a large number of high speed digital signals while managing electrical noise. The ability to offer wideband data converters with GSPS sampling frequencies, using fewer interconnects, simplifies the PCB layout challenges and allows for smaller form factor realization without impacting overall system performance.

Market forces continue to press for more features, functionality, and performance in a given system, driving the need for higher data-handling capacity. The high speed analog-to-digital converter and digital-to-analog converter-to-FPGA interface had become a limiting factor in the ability of some system OEMs to meet their next generation data-intensive demands. The JESD204B serial interface specification was specifically created to help solve this problem by addressing this critical data link. Figure 1 shows typical high speed converter-to-FPGA interconnect configurations using JESD204A/JESD204B.

Some key end-system applications that are driving the deployment of this specification, as well as a contrast between serial LVDS and JESD204B, are the subject of the remainder of the article.

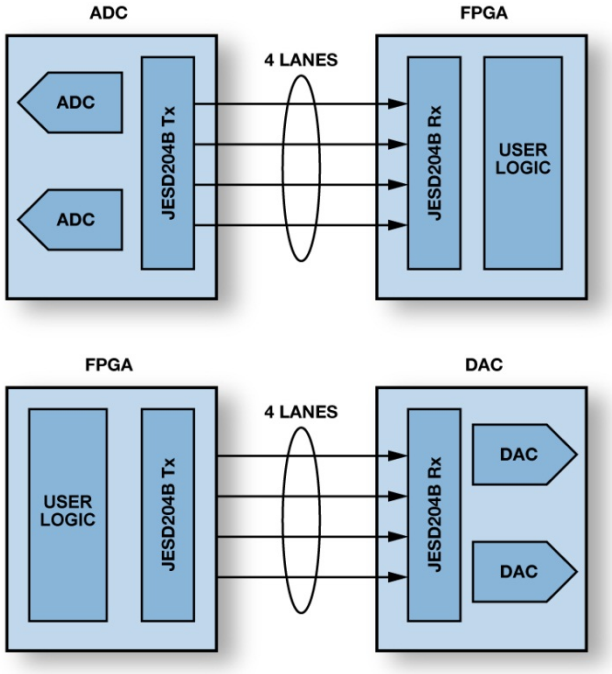


Figure 1. Typical High Speed Converter to FPGA Interconnect Configurations Using JESD204A/JESD204B Interfacing (Source: Xilinx)

THE APPLICATIONS DRIVING THE NEED FOR JESD204B

Wireless Infrastructure Transceivers

OFDM based technologies, such as LTE, used in today's wireless infrastructure transceivers use DSP blocks implemented on FPGAs or SoC devices driving antenna array elements to generate beams for each individual subscriber's handset. Each array element can require movement of hundreds of megabytes of data per second between FPGAs and data converters in both transmit or receive modes.

Software Defined Radios

Today's software defined radios utilize advanced modulation schemes that can be reconfigured on the fly, and rapidly increasing channel bandwidths, to deliver unprecedented wireless data rates. Efficient, low power, low pin count FPGA-to-data converter interfaces in the antenna path play a critical role in their performance. Software defined radio architectures are integral to the transceiver infrastructure

for multicarrier, multimode wireless networks supporting GSM, EDGE, W-CDMA, LTE, CDMA2000, WiMAX, and TD-SCDMA.

Medical Imaging Systems

Medical imaging systems including ultrasound, computational tomography (CT) scanners, magnetic resonance imaging (MRI), and others generate many channels of data that flow through a data converter to FPGAs or DSPs. Continually increasing I/O counts are driving up the number of components by requiring the use of interposers to match FPGA and converter pin out and increasing PCB complexity. This adds additional cost and complexity to the customer's system that can be solved by the more efficient JESD204B interface.

Radar and Secure Communications

Increasingly sophisticated pulse structures on today's advanced radar receivers are pushing signal bandwidths toward 1 GHz and higher. Latest generation active electronically scaled array (AESA) radar systems may have thousands of elements. High bandwidth SERDES-based serial interfaces are needed to connect the array element data converters to the FPGAs or DSPs that process incoming and generate outgoing data streams.

SERIAL LVDS VS. JESD204B

Choosing Between Series LVDS and JESD204B Interface

In order to best select between converter products that use either LVDS or the various versions of the JESD204 serial interface specification, a comparison of the features and capabilities of each interface is useful. A short tabular comparison is provided in Table 1. At the SerDes level, a notable difference between LVDS and JESD204 is the lane data rate, with JESD204 supporting greater than three times the serial link speed per lane when compared with LVDS. When comparing the high level features like multidevice synchronization, deterministic latency, and harmonic clocking, JESD204B is the only interface that provides this functionality. Systems requiring wide bandwidth multichannel converters that are sensitive to deterministic latency across all lanes and channels won't be able to effectively use LVDS or parallel CMOS.

Table 1. Comparison Between Serial LVDS and JESD204 Specifications

Function	Serial LVDS	JESD204	JESD204A	JESD204B
Specification Release	2001	2006	2008	2011
Maximum lane Rate	1.0 Gbps	3.125 Gbps	3.125 Gbps	12.5 Gbps
Multiple Lanes	No	No	Yes	Yes
Lane Synchronization	No	No	Yes	Yes
Multidevice Synchronization	No	Yes	Yes	Yes
Deterministic Latency	No	No	No	Yes
Harmonic Clocking	No	No	No	Yes

LVDS OVERVIEW

Low voltage differential signaling (LVDS) is the traditional method of interfacing data converters with FPGAs or DSPs. LVDS was introduced in 1994 with the goal of providing higher bandwidth and lower power dissipation than the existing RS-422 and RS-485 differential transmission standards. LVDS was standardized with the publication of TIA/EIA-644 in 1995. The use of LVDS increased in the late 1990s and the standard was revised with the publication of TIA/EIA-644-A in 2001.

LVDS uses differential signals with low voltage swings for high speed data transmission. The transmitter typically drives ±3.5 mA with a polarity matching the logic level to be sent through a 100 Ω resistor, generating a ±350 mV voltage swing at the receiver. The always-on current is routed in different directions to generate logic ones and zeros. The always-on nature of LVDS helps eliminate simultaneous switching noise spikes and potential electromagnetic interference that sometimes occur when transistors are turned on and off in single-ended technologies. The differential nature of LVDS also provides considerable immunity to common-mode noise sources. The TIA/EIA-644-A standard recommends a maximum data rate of 655 Mbps, although it predicts a possible speed of over 1.9 Gbps for an ideal transmission medium.

The huge increase in the number and speed of data channels between FPGAs or DSPs and data converters, particularly in the applications described earlier, has created several issues with the LVDS interface (see Figure 2). The bandwidth of a differential LVDS wire is limited to about 1.0 Gbps in the real world. In many current applications, this creates the need for a substantial number of high bandwidth PCB interconnects, each of which is a potential failure point. The large number of traces also increases PCB complexity or overall form

factor, which raises both design and manufacturing costs. In some applications, the data converter interface becomes the limiting factor in achieving the required system performance in bandwidth hungry applications.

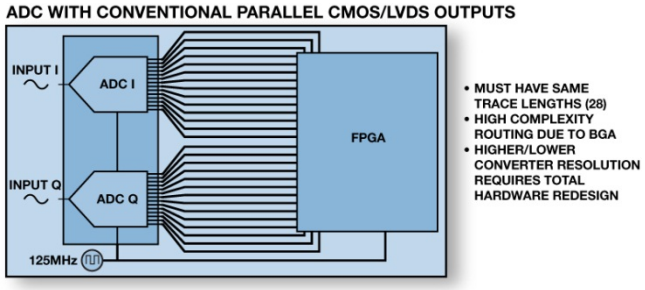


Figure 2. Challenges in System Design and Interconnect Using Parallel CMOS or LVDS

JESD204B OVERVIEW

The JESD204 data converter serial interface standard was created by the JEDEC Solid State Technology Association JC-16 Committee on Interface Technology with the goal of providing a higher speed serial interface for data converters to increase bandwidth and reduce the number of digital inputs and outputs between high speed data converters and other devices. The standard builds on 8b/10b encoding technology developed by IBM that eliminates the need for a frame clock and a data clock, enabling single line pair communications at a much higher speed.

In 2006, JEDEC published the JESD204 specification for a single 3.125 Gbps data lane. The JESD204 interface is self-synchronous, so there is no need to calibrate the length of the PCB wire traces to avoid clock skew. JESD204 leverages the SerDes ports offered on many FPGAs to free up general-purpose I/O.

JESD204A, published in 2008, adds support for multiple time-aligned data lanes and lane synchronization. This enhancement makes it possible to use higher bandwidth data converters and multiple synchronized data converter channels and is particularly important for wireless infrastructure transceivers used in cellular base stations. JESD204A also provides multidevice synchronization support which is useful for devices, such as medical imaging systems, that use large numbers of ADCs.

JESD204B, the third revision of the spec, increases the maximum lane rate to 12.5 Gbps. JESD204B also adds deterministic latency, which communicates synchronization status between the receiver and transmitter. Harmonic clocking, also introduced in JESD204B, makes it possible to derive a high speed data converter clock from a lower speed input clock with deterministic phasing.

SUMMARY

The JESD204B industry serial interface standard reduces the number of digital inputs and outputs between high speed data converters and FPGAs and other devices. Fewer interconnects simplify layout and make it possible to achieve a smaller form factor (see Figure 3). These advantages are important for a wide range of high speed data converter applications, such as wireless infrastructure transceivers, software defined radios, medical imaging systems, and radar and secure communications. Analog Devices, Inc., is an original participating member of the JESD204 standards committee and we have concurrently developed compliant data converter technology and tools along with a comprehensive product roadmap offering. By providing customers with products that combine our cutting edge data converter technology along with the JESD204A/JESD204B interface, we expect to enable customers to solve their system design problems, while taking advantage of this significant interfacing breakthrough.

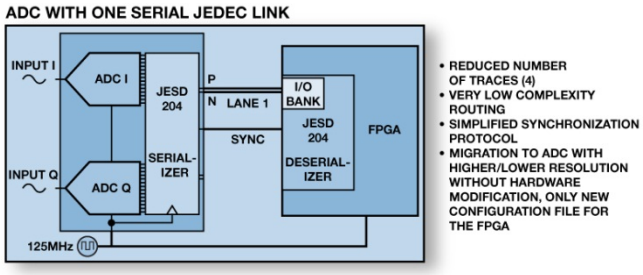


Figure 3. JESD204 with Its High Speed Serial I/O Capability Solves the System PCB Complexity Challenge

ABOUT THE AUTHOR

George Diniz is a Product Line Manager in the High Speed Digital-to-Analog Converters Group at Analog Devices in Greensboro, NC. He leads a team responsible for the development of JESD204B Rx and Tx interface cores, which are integrated into high speed analog-to-digital and digital-to-analog converter products. He has 25 years of experience in the semiconductor industry and has held various roles in design engineering and product line management. Before joining ADI, George was a design engineer at IBM, where he was engaged in mixed-signal design of custom SRAM macros, PLL, and DLL functions for PowerPC processors. He has an MSEE from North Carolina State University and a BEE from Manhattan College. For recreation, George enjoys outdoor activities, restoring automobiles, and running.

RESOURCES

Share this article on  

One Technology Way • P.O. Box 9106 • Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 • Fax: 781.461.3113 • www.analog.com

TA11326-0-1/13

ANALOG DEVICES

Grasp the Critical Issues for a Functioning JESD204B Interface

by Anthony Desimone, Applications Engineer, Analog Devices, Inc., and Michael Giancioppo, Applications Engineer, Analog Devices.

JESD204B is a recently approved JEDEC Standard for serial data interfacing between converters and digital processing devices. As a third-generation standard, it addresses some of the limitations of the earlier versions. Among the benefits of this interface are reductions in required board area for data interface routing, reductions in setup and hold timing requirements, and the enablement of smaller packages for converter and logic devices. New analog/digital converters from various vendors, such as the AD9250 from Analog Devices, Inc., use this interface.

There is a trade-off to realizing the benefits of the JESD204B interface, as it has complexities and subtleties which distinguish it from existing interface formats and protocols. As with any standard, it is clear that the interface must function seamlessly to gain popularity and traction versus more common interfaces, such as single data rate or double data rate CMOS or LVDS. Although the JESD204B standard is documented by JEDEC, some specific information about it is subject to interpretation or may be spread over multiple references. It is also obvious that it would be extremely helpful if there were a concise guide that provided an overview of the standard, how it works, and how to troubleshoot it if issues arise.

This article explains the interface from an ADC to FPGA for JESD204B, how to identify when it's working correctly, and, perhaps more important, how to troubleshoot it if something isn't quite right. The troubleshooting techniques discussed can use commonly available test and measurement equipment including oscilloscopes and logic analyzers, along with software tools such as the ChipScope from Xilinx® or SignalTap from Altera®. Interface signaling is also explained to allow a single approach or multiple approaches to visualize the signaling.

JESD204B OVERVIEW

The JESD204B standard provides a method to interface one or multiple data converters to a digital-signal processing device (typically, an ADC or DAC to an FPGA) over a higher speed serial interface compared to the more typical parallel data transfers. The interface, which runs at up to 12.5 Gbps/lane, uses a framed serial data link with embedded clock and alignment characters. The interface eases implementation of the data interface of high speed converters by reducing the number of traces between devices, thus reducing trace-matching requirements, and removing setup- and hold-timing constraint issues. Since a link needs to be established prior to data transfer, there are new challenges and techniques required to identify that the interface is working properly and, if not, what to do.

Starting with a brief explanation of how the standard works, the JESD204B interface uses three phases to establish the synchronized link: code group synchronization (CGS), initial lane synchronization (ILAS), and data transmission phase. Required signals for the link are a shared reference clock (device clock), at least one differential CML physical data electrical connection (called a lane), and at least one other synchronization signal (SYNC~ and possibly SYSREF). The signals used depend upon the subclass:

- Subclass 0 uses device clock, lanes, and SYNC~
- Subclass 1 uses device clock, lanes, SYNC~, and SYSREF
- Subclass 2 uses device clock, lanes, and SYNC~

Subclass 0 is adequate in many cases and will be the focus of this article. Subclass 1 and Subclass 2 provide a method to establish deterministic latency. This is important in application when synchronizing multiple devices or system synchronization or fixed latency is required (such as when a system needs a known sampling edge for an event or an event must react to an input signal within a specified time).

Figure 1 shows a simplified JESD204B link from the Tx device (ADC) to the Rx device (FPGA), with data from one ADC going over one lane.

Although there are many variables within the JESD204B specification, some have particular importance when establishing a link. These key variables from the specification are (note that these values are typically represented as "X – 1"):

- M: number of converters.
- L: number of physical lanes.
- F: number of octets per frame.
- K: number of frames per multiframe.
- N and N': converter resolution and number of bits used per sample (multiple of 4), respectively. N' value is N value, plus control and dummy bits.

SUBCLASS 0: SYNCHRONIZATION STEPS

As noted above, many applications can use the relatively simpler Subclass 0 mode of operation. This is also the easiest mode to establish and for which to verify a link. Subclass 0 uses three phases to establish and monitor synchronization: CGS phase, ILAS phase, and data phase. The figures associated with each phase present the data in different formats, as they might be seen on an oscilloscope, logic analyzer, or FPGA virtual I/O analyzer such as Xilinx ChipScope or Altera SignalTap.

The Code Group Synchronization (CGS) Phase

The most significant parts of the CGS phase that can be observed over the link are shown in Figure 2, along with a description of the five highlighted points of the figure.

1. The Rx issues a synchronization request by driving the SYNC~ pin low.
2. The Tx transmits /K28.5/ symbols (10 bits/symbol), unscrambled beginning on the next symbol.
3. The Rx synchronizes when it receives at least four consecutive /K28.5/ symbols without error and then the Rx drives the SYNC~ pin high.
4. Rx must receive at least four 8B/10B characters without error otherwise synchronization fails and the link stays in CGS phase.
5. CGS Phase ends and ILAS phase begins.

The /K28.5/ character, also just known as /K/, within the JESD204B standard can be exhibited as shown in Figure 3. The standard requires a running neutral disparity. The 8B10B coding allows a balanced sequence that, on average, contains an equal amount of 1's and 0's. Each 8B10B character can have a positive (more 1's) or negative (more 0's) disparity, and the parity of the current character is determined by the current sum of the previous characters sent, and this is typically accomplished by alternately transmitting a positive parity word, followed by a negative parity word; the figure shows both polarities of the /K28.5/ symbol.

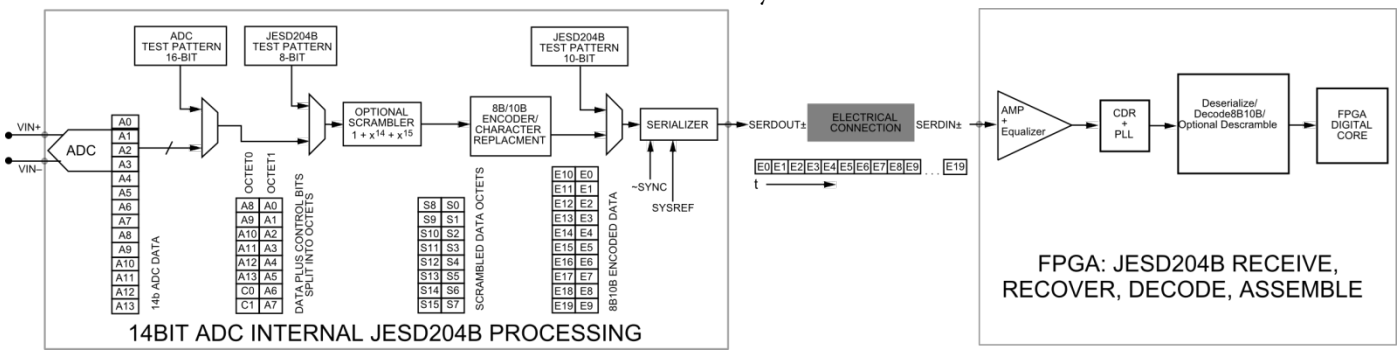


Figure 1. JESD204B Link Diagram for One ADC to an FPGA through One Lane

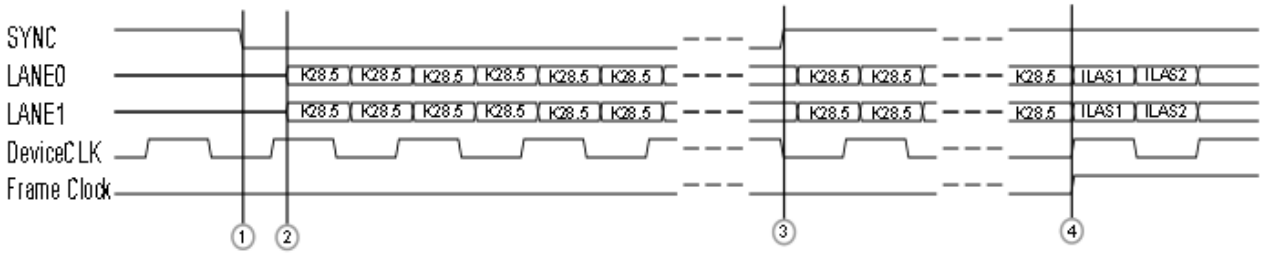


Figure 2. Logic Output of JESD204B Subclass 0 Link Signals During CGS Phase (Assumes Two Lanes, One Device with Two ADCs)

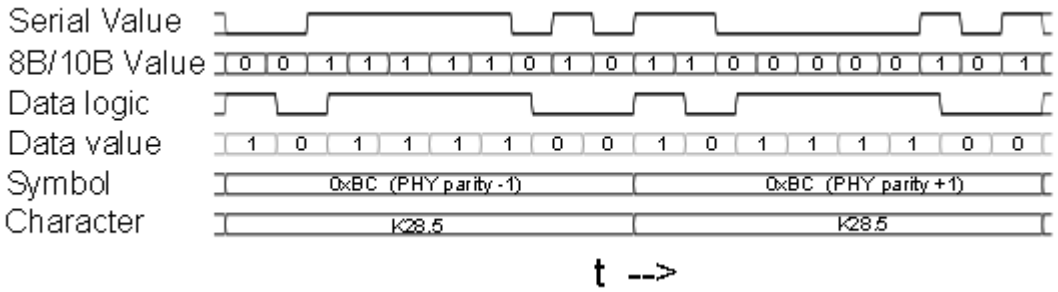


Figure 3. Logic Output of /K28.5/ Characters and How It Propagates through the JESD204B Tx Signal Path

Note these key points:

- *Serial Value* represents the logic levels of the 10 bits transmitted over the lane, as would be seen by an oscilloscope measuring the physical interface.
- *8B/10B Value* represents the logic values (10 bits) transmitted over the lane, as might be seen by a logic analyzer measuring the physical interface.
- *Data value* and *Data logic* represent the logic levels of the symbol inside the JESD204B Tx block before 8B10B coding, as would be seen on an FPGA logic analysis tool such as Xilinx ChipScope or Altera SignalTap.
- *Symbol* represents the hex value of the character that is to be transmitted, noting parity for PHY layer
- *Character* is shown to indicate the JESD204B character as it is referred to in the JEDEC specification.

THE ILAS PHASE

In the ILAS phase, there are four multiframes which allow the Rx to align lanes from all links and also allows the Rx to verify the link parameters. Alignment is required to accommodate trace length differences and any character skew the receivers introduce. Each successive multiframe immediately follows the previous one of four (Figure 4). Whether or not the scrambling link parameter is enabled, ILAS is always transmitted without scrambling.

The ILAS phase begins after SYNC~ has been deasserted (goes high). After the transmit block has internally tracked (within the ADC) a full multiframe, it will begin to transmit four multiframes. Dummy samples are inserted between the required characters so that full multiframes are transmitted (Figure 4). The four multiframes consist of the following:

- Multiframe 1: begins with an /R/ character [K28.0] and ends with an /A/ character [K28.3].
- Multiframe 2: begins with an /R/ character followed by a /Q/ [K28.4] character, followed by link configuration parameters over 14 configuration octets (Table 1), and ends with an /A/ character.
- Multiframe 3: the same as Multiframe 1.
- Multiframe 4: the same as Multiframe 1.

The frame length can be calculated for the JESD204B parameters: (S) × (1/Sample Rate).

> Translation: (Number of Samples / Converter / Frame) × (1/Sample Rate)
>
> Example: a converter that has one sample per converter per frame (Note "S" is 0 in this case since it is encoded as Binary value –1) and the converter is running at 250 MSPS has a 4 ns frame length
>
> (1) × (1/250 MHz) = 4 ns

The multiframe length can be calculated for the JESD204B parameters: K × S × (1/Sample Rate)

> Translation: (Number of Samples / Converter / Frame) × (Number of Frames / Multiframe) × (1/Sample Rate)
>
> Example: a converter that has one sample per converter per frame, 32 frames per multiframes, and the converter running at 250 MSPS has a 128 ns multiframe length
>
> (1) × (32) × (1/250 MHz) = 128 ns

DATA PHASE WITH CHARACTER REPLACEMENT ENABLED

In the data transmission phase, frame alignment is monitored with control characters. Character replacement is used at the end of frames. There is no additional overhead to accommodate data or frame alignment during the data phase. Character replacement allows an alignment character to be issued at a frame boundary "if and only if" the last character of the current frame may be replaced with the last character of the last frame, facilitating (occasional) confirmation that the alignment has not changed since the ILAS sequence.

Character replacement in the transmitter occurs in the following instances:

- If scrambling is disabled and the last octet of the frame or multiframe equals the octet value of the previous frame.
- If scrambling is enabled and the last octet of the multiframe is equal to 0x7C, or the last octet of a frame is equal to 0xFC.

Transmitters and receivers each maintain a multiframe counter (LMFC) that perpetually count to (F × K) − 1 and then wrap back to "0" to count again (ignoring internal word width). A common (sourced) SYSREF is issued to all transmitters and receivers which use the SYSREF to reset their LMFCs, after which all LMFCs should be synchronized (within one clock) to each other.

At the release of SYNC (seen by all devices) the transmitter begins ILAS at the next (Tx) LMFC wrap to "0". If F × K has been properly set to be greater than the (transmit encode time) + (line propagation time) + (receiver decode time), received data will propagate out of the receiver's SerDes before the next LMFC. The receiver will pass the data into a FIFO, which will begin outputting data at the next (Rx) LMFC boundary. This "known relationship" between the transmitter's SerDes input and the receiver's FIFO output are known as the "deterministic latency".

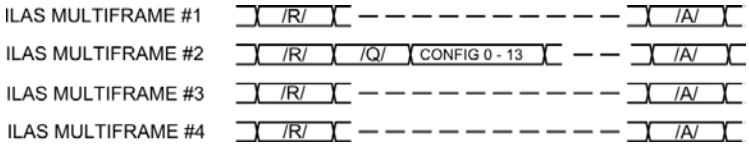


Figure 4. Logic Output of JESD204B Subclass 0 Link Signals During ILAS Phase

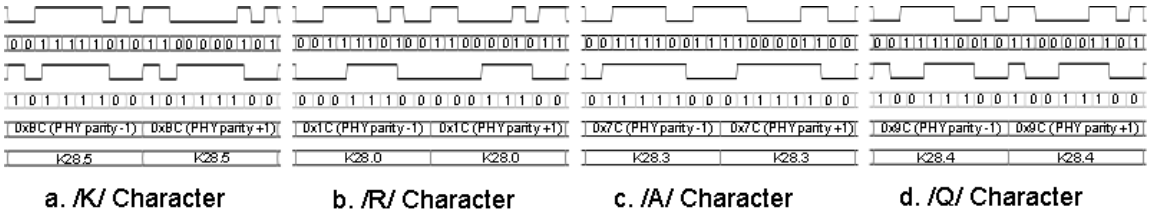


Figure 5. Figure of /K/ Character [K28.5], /R/ Character [K28.0], /A/ Character [K28.3], and /Q/ character [K28.4]

Table 1. Table of CONFIG (Fourteen JESD204B Configuration Parameters Octets) in ILAS Multiframe 2

Octet No.	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
0	DID[7:0]							
1	ADJCNT[3:0]				BID[3:0]			
2		ADJDIR	PHADJ	LID[4:0]				
3	SCR			L[4:0]				
4	F[7:0]							
5				K[4:0]				
6	M[7:0]							
7	CS[1:0]			N[4:0]				
8	SUBCLASS[2:0]			N[4:0]				
9	JESDV[2:0]			S[4:0]				
10	HD			CF[4:0]				
11	RESERVED 1							
12	RESERVED 2							
13	FCHK[7:0]							

WHAT CAN GO WRONG?

JESD204B can be a complicated interface standard, with many operational subtleties. Finding out why it is not working requires a good understanding of likely scenarios:

Stuck in CGS mode: if SYNC stays at logic low level; or pulse high for <4 multiframes:

1. Checking the board, unpowered:
   a) SYSREF and SYNC~ signaling should be dc coupled.
   b) With the board unpowered, check that the board SYNC~ connections from the SYNC~ source (typically from the FPGA or DAC) to the SYNC~ input (typically ADC or FPGA) are good and low impedance.
   c) Check that the pull-down or pull-up resistors are not dominating the signaling, for example, if values are too small or shorted and, therefore, cannot be driven correctly.
   d) Verify that the differential-pairs traces (and cables, if used) of JESD204B link are matched.
   e) Verify differential impedance of the traces is 100 Ω.
2) Checking the board, powered:
   a) If there is a buffer/translator in the SYNC path, make sure it is functioning properly.
   b) Check that SYNC~ source and board circuitry (both SYNC+ and SYNC–, if differential) are properly configured to produce logic levels compliant for the SYNC~ receive device. If logic level is not compliant, then review circuitry for source and receive configurations to find the problem. Otherwise, consult device manufacturer.
   c) Check that the JESD204B serial transmitter and board circuitry are properly configured to produce the correct logic levels for the JESD204B serial data receiver. If logic level is not compliant review circuitry of source and receive configurations to find the problem. Otherwise, consult device manufacturer.
3) Checking SYNC~ signaling:
   a) If SYNC~ is static and logic low, the link is not progressing beyond the CGS phase. There is either an issue with the data being sent, or the JESD204B receiver is not decoding the samples properly. Verify /K/ characters are being sent, verify receive configuration settings, verify SYNC~ source, review board circuitry, and consider overdriving SYNC~ signal and attempt to force link into ILAS mode to isolate link Rx vs. Tx issues. Otherwise, consult device manufacturer.
   b) If SYNC~ is static and logic high, verify the SYNC~ logic level is configured correctly in the source device. Check pull-up and pull-down resistors.
   c) If SYNC~ pulses high and returns to logic-low state for less than six multiframe periods, the JESD204B link is progressing beyond the CGS phase but not beyond ILAS phase. This would suggest the /K/ characters are okay and the basic function of the CDR are working. Proceed to the ILAS troubleshooting section.
   d) If SYNC~ pulses high for a duration of more than six multiframe periods, the link is progressing beyond the ILAS phase and is malfunctioning in the data phase; see the data phase section for troubleshooting tips.
4) Checking serial data
   a) Verify the Tx data rate and the receiver's expected rate are the same.
   b) Measure lanes with high impedance probe (differential probe, if possible); if characters appear incorrect, make sure lane differential traces are matched, the return path on the PCB is not interrupted, and devices are properly soldered on the PCA. Unlike the (seemingly) random characters of ILAS and data phase, CGS characters are easily recognizable on a scope (if a high enough speed scope is available).
   c) Verify /K/ characters with high impedance probe.
      i) If /K/ characters are correct, the Tx side of the link is working properly.
      ii) If /K/ characters are not correct, the Tx device or the board Lanes signal have an issue.
   d) If dc coupled, verify that the transmitter and receiver common-mode voltage is within specification for the devices
      i) Depending upon implementation, the transmitter common-mode voltage can range from 490 mV to 1135 mV.
      ii) Depending upon implementation, the receiver common-mode voltage can range from 490 mV to 1300 mV.

e) Verify the transmitter CML differential voltage on the data lanes (note that the CML differential voltage is calculated as two times the voltage swing of each leg of the signal).
   i) The transmitter CML differential voltage can range from 0.5 Vpk-pk to 1.0 Vpk-pk for speeds up to 3.125 Gbps.
   ii) The transmitter CML differential voltage can range from 0.4 Vpk-pk to 0.75 Vpk-pk for speeds up to 6.374 Gbps.
   iii) The transmitter CML differential voltage can range from 0.360 Vpk-pk to 0.770 Vpk-pk for speeds up to 12.5 Gbps.

f) Verify the receiver CML differential voltage on the data lanes (note that the CML differential voltage is calculated as two times the voltage swing of each leg of the signal).
   i) The receiver CML differential voltage can range from 0.175 Vpk-pk to 1.0 Vpk-pk for speeds up to 3.125 Gbps.
   ii) The receiver CML differential voltage can range from 0.125 Vpk-pk to 0.75 Vpk-pk for speeds up to 6.374 Gbps.
   iii) The receiver CML differential voltage can range from 0.110 Vpk-pk to 1.05 Vpk-pk for speeds up to 12.5 Gbps.

g) If preemphasis is an option, enable and observe data signals along the data path.

h) Verify that the M and L values match between the transmitter and receiver, otherwise the data rates may not match. For example, M = 2 and L= 2 will expect ½ the data rate over the serial interface as compared to the M = 2 and L = 1 case.

i) Ensure the device clock going to the transmitter and receiver is phase locked and at the correct frequency.

Can not get beyond ILAS mode if SYNC pulses high for approximately four multiframes:

1) Link parameter conflicts
   a) Verify link parameters are not offset by 1 (many parameters are specified as value −1)
   b) Verify ILAS multiframes are transmitting properly, verify link parameters on the Tx device, the Rx device, and those transmitted in ILAS second multiframe.
   c) Calculate expected ILAS length (t_{frame}, $t_{multiframe}$, 4 × $t_{multiframe}$), verify ILAS is attempted for approximately four multiframes.
2) Verify all lanes are functioning properly. Ensure there are no multilane/multilink conflicts.

Get into data phase but occasionally link resets (returns to CGS and ILAS before returning to data phase):

1) Invalid setup and hold time of periodic or gapped periodic SYSREF or SYNC~ signal.
2) Link parameter conflicts.
3) Character replacement conflicts.
4) Scrambling problem, if enabled.
5) Lane data corruption, noisy or jitter could force the eye diagram to close.
6) Spurious clocking or excessive jitter on device clock.

Other general tips when troubleshooting link:

- Run converter and link at slowest allowed speed, as this allows use of lower-bandwidth measurement instruments that are more readily available.
- Set minimum allowed combinations of M, L, K, S.
- Use test modes when possible.
- Use Subclass 0 for troubleshooting.
- Disable scrambling while troubleshooting.

This troubleshooting guide cannot be all inclusive but provides a good basic baseline for an engineer working with and wanting to learn about a JESD204B link.

This summary of the JESD204B specification provides practical information about the link. Hopefully, engineers getting involved with this latest high performance interface standard will find it informative and helpful if troubleshooting is required.

ABOUT THE AUTHOR

Anthony Desimone is an application engineer in the High Speed Converter Group at Analog Devices. He has a BSEE from the University of Lowell (Massachusetts) and an MSEE from Tufts University.

Michael Giancioppo is an application engineer in the Applications Technology Group at Analog Devices. He received a BSEE/CSE from the University of Massachusetts Amherst in 1981.

RESOURCES

Share this article on  

One Technology Way • P.O. Box 9106 • Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 • Fax: 781.461.3113 • www.analog.com

TA11327-0-10/13(A)

Synchronizing Multiple ADCs Using JESD204B

by Ian Beavers, Applications Engineer, Analog Devices, Inc.

IDEA IN BRIEF

Many communications, instrumentation, and signal acquisition systems require the ability to simultaneously sample analog input signals across multiple analog-to-digital converters (ADC). The sampled data then needs to be processed with the expectation of synchronization across these inputs that each have their own various different latencies. This has historically been a difficult challenge for system designers to meet with LVDS and parallel output ADCs.

JESD204B provides a framework for high speed serial data to be sent along one or more differential signal pairs, such as an output of an ADC. There is an inherent scheme in the interface to achieve coarse alignment across lanes within the JESD204B specification. Data is partitioned into frames with boundaries that are continuously sent to the receiver. The JESD204B Subclass 1 interface has provisions for data alignment down to the sample level across multiple serial lane links or multiple ADCs by using a system reference event signal (SYSREF) to synchronize internal framing clocks in both the transmitter and receiver. This creates a deterministic latency for the devices using the JESD204B link. However, there are still many challenges that a system designer must overcome to achieve full timing closure for sampling synchronization, such as PCB layout considerations, matched clock, and SYSREF generation to meet timing, SYSREF periodicity, and digital FIFO delays.

The designer must decide how the device clock and SYSREF signal will be created and distributed throughout the system. Ideally, the device clock and SYSREF should be of the same swing level and offset to prevent inherent skew at the component input pin. The update rate of the SYSREF event will need to be determined as either a single event at startup or a recurring signal that may occur at any time synchronization is needed. Taking the maximum clock and SYSREF signal skew into consideration, careful PCB layout is needed to meet setup and hold timing across boards, connectors, backplanes, and various components. Finally, digital FIFO design and signals traversing across multiple clock domains create inherent digital buffer skew within JESD204B transmitters and receivers that must be accounted for and removed in back-end data processing.

System clock generation can come from several sources such as crystals, VCOs, and clock generation or clock distribution chips. While the particular system performance will dictate the clocking needs, one, using multiple synchronous ADCs, must be able to produce a SYSREF signal that is source synchronous to the input clock. This makes the clock source selection an important consideration in order to be able to latch this system reference event with a known clock edge at a particular point in time. If the SYSREF signal and clock are not phased locked, this cannot be achieved.

An FPGA can be used to provide a SYSREF event to the system. However, unless it also uses and synchronizes to the master sample clock that is sent to the ADCs, it will be difficult to phase align the SYSREF signal from the FPGA to the clock. An alternate approach is to provide the SYSREF signal from a clock generation or clock distribution chip that can phase align this signal to multiple clocks that are sent throughout the system. Using this method, the SYSREF event can be a one shot event at startup, or a recurring signal depending upon the system requirements.

As long as deterministic latency remains constant within the system across ADCs and FPGAs, additional SYSREF pulses may not be needed except to help frame particular system data. Hence, a periodic SYSREF pulse for clock alignment can be ignored or filtered until the time at which synchronization is lost. A marker sample for the occurrence of SYSREF could alternately be maintained without resetting the JESD204B link.

In order to initiate a known deterministic starting point for the ADC channels, the system engineer must be able to close timing for the SYSREF event signal distributed across the system. This means that the expected setup and hold time, relative to the clock, must be met without violation. Use of a relatively long SYSREF pulse that spans multiple clock cycles can be used to meet the hold time requirement, so long as the setup time to the first required clock can also be met. Careful attention to PCB layout is critical in this effort to maintain matched trace lengths for clocks and SYSREF within the system for minimum skew. This may be the most difficult part of achieving synchronous sampling processing across channels. The effort will only get progressively more

challenging as ADC encode clock rates increase and multiboard systems become more complex.

SYSREF to clock board skew at components across boards and connectors must be deterministically known for each device by the system engineer. Any remaining inter-device digital and clock skew delays need to be effectively nulled in the FPGA or ASIC. Back-end processing can change the sample order across ADCs and introduce any needed re-alignment to prepare the data for further synchronized processing. Correction for inter-device sample skew can be accomplished by delaying the fastest data samples and transmitter latency to align with the slowest data samples in the back-end FPGA or ASIC. For complex systems, this may involve multiple FPGA or ASIC where each needs to communicate their total inter-device sample latency for final alignment. By introducing appropriate elastic buffer delays in the JESD204B receiver(s) to accommodate each specific transmitter latency delay, the inter-device sample skews can be aligned with known determinism across a system.

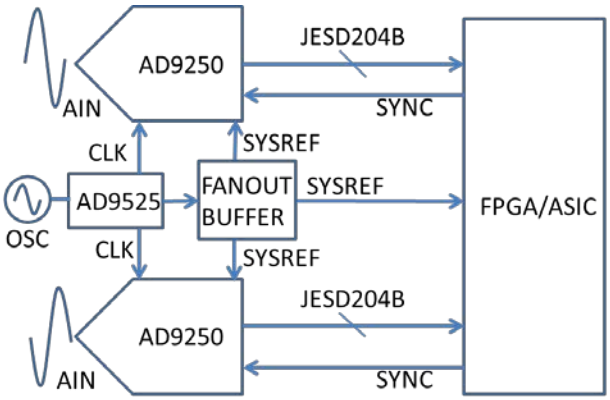


Figure 1. Diagram Showing the AD9250, the AD9525, and FPGA

The AD9250 is a 250 MSPS 14-bit dual ADC from Analog Devices, Inc., that supports the JESD204B interface in a Subclass 1 implementation. This subclass allows analog sample synchronization across ADCs using the SYSREF event signal. The AD9525 is a low jitter clock generator that not only provides seven clock outputs up to 3.1 GHz but is also able to synchronize a SYSREF output signal based on user configurations. These two products, coupled with a selection of fanout buffer products from Analog Devices, provide the framework to accurately synchronize and align multiple ADC data sent to an FPGA or ASIC for processing.

ABOUT THE AUTHOR

Ian Beavers is an applications engineer for the High Speed Converter Group at Analog Devices, Inc. (Greensboro, NC). He has worked for the company since 1999. Ian has over 15 years of experience in the semiconductor industry. He earned a bachelor's degree in electrical engineering from North Carolina State University and an MBA from the University of North Carolina at Greensboro. He can be reached at Ian.Beavers@analog.com.

RESOURCES

Share this article on

One Technology Way • P.O. Box 9106 • Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 • Fax: 781.461.3113 • www.analog.com
Trademarks and registered trademarks are the property of their respective owners. TA11325-0-1/13

Three Key Physical Layer (PHY) Performance Metrics for a JESD204B Transmitter

by Jonathan Harris, Applications Engineer, Analog Devices, Inc.

INTRODUCTION

With the increased adoption of the JESD204 interface in data converters, it has become necessary to devote more attention to the performance and optimization of the digital interface. The focus must not be only on the data converter performance. The first two revisions of the standard, JESD204 in 2006 and JESD204A in 2008, specified data rates of 3.125 Gbps. The latest revision, JESD204B released in 2011, lists three speed grades with the maximum data rate of 12.5 Gbps. These three speed grades are governed by three different electrical interface specifications formulated by the Optical Internetworking Forum (OIF). For data rates up to 3.125 Gbps, OIF-Sx5-01.0, details the electrical interface specifications while the CEI-6G-SR and CEI-11G-SR detail the specifications for data rates up to 6.375 Gbps and 12.5 Gbps, respectively. The high speed data rates require more attention be given to the design and performance of the high speed CML drivers, receivers, and interconnect network which make up the physical interface (PHY) of the JESD204B interface.

To evaluate the performance of the PHY for a JESD204B transmitter, there are several performance metrics that are evaluated. These include common-mode voltage, differential peak-to-peak voltage, differential impedance, differential output return loss, common-mode return loss, transmitter short circuit current, eye diagram mask, and jitter. This article will focus on three key performance metrics that are typically used to evaluate the quality of the transmitted signal, the eye diagram, the bathtub plot, and the histogram plot. These measurements are made from the perspective of the receiver as that is where the signal must be properly decoded. The eye diagram overlays multiple acquisitions of the output data transitions to create a plot that can give many indications of the link quality. This plot can be used to observe many characteristics of the JESD204B physical interface such as impedance discontinuities and improper terminations. This is just one way that the physical layer can be evaluated. The bathtub plot and the histogram plot are two other important performance metrics that are used to evaluate the quality of the JESD204B link. The bathtub plot gives a visual representation of the bit error rate (BER) for a given eye width opening, measured in terms of the unit interval (UI). The unit interval is the specified time given in the physical layer specifications for JESD204B that gives the amount of time between data transitions. The third measurement is the histogram plot which gives the distribution of the measured UI variation. The measurement is also an indication of the amount of jitter present in the measured signal. This plot, along with the eye diagram and the bathtub plot, can be used to gauge the overall performance of the physical layer of the JESD204B interface. A JESD204B transmitter with an output data rate of 5.0 Gbps is presented. The performance for a transmitter of this data rate is detailed by the OIF CEI-6G-SR specification.

THE EYE DIAGRAM

Figure 1 shows an eye diagram for a JESD204B transmitter with a 5.0 Gbps data rate. The ideal waveform is overlaid on a measured waveform. Ideally, the transitions would be almost instantaneous with no overshoot or undershoot and without any ringing. In addition, the cross points which determine the UI would be without jitter. As can be seen from Figure 1, in a real system, ideal waveforms are not possible to achieve due to nonideal transmission media which has loss and terminations that are not matched exactly. The eye diagram shown is a measurement made at the receiver in a JESD204B system. The signal has passed through a connector and approximately 20 cm of differential transmission lines before making it to the measurement point. This eye diagram indicates a reasonable impedance match between the transmitter and receiver and a good transmission media with no large impedance discontinuities. It does exhibit an amount of jitter but not in excess of the specifications for the JESD204 interface. The eye diagram does not exhibit any overshoot but does have a slight amount of undershoot on the rising edges due to the slowing of the signal as it passes through the transmission media. This is to be expected, however, after passing through the connector and the 20 cm of differential transmission lines. The mean UI looks to match the expected UI of approximately 200 ps with the signal having a small amount of jitter. Overall, this eye diagram presents a good signal to the receiver which

should have no trouble recovering the embedded data clock and properly decoding the data.

The eye diagram presented in Figure 2 is measured with the same transmission media used in the measurement for Figure 1, with the exception that the termination impedance is incorrect. The effects can be seen in the increased amount of jitter present in the signal at the crossing points, as well as in the nontransition areas. The overall amplitude is compressed in many of the data acquisitions resulting in an eye diagram that is beginning to close. The degradation will cause an increase in the BER at the receiver and could possibly result in the loss of the JESD204B link at the receiver if the eye closes beyond what the receiver can tolerate.

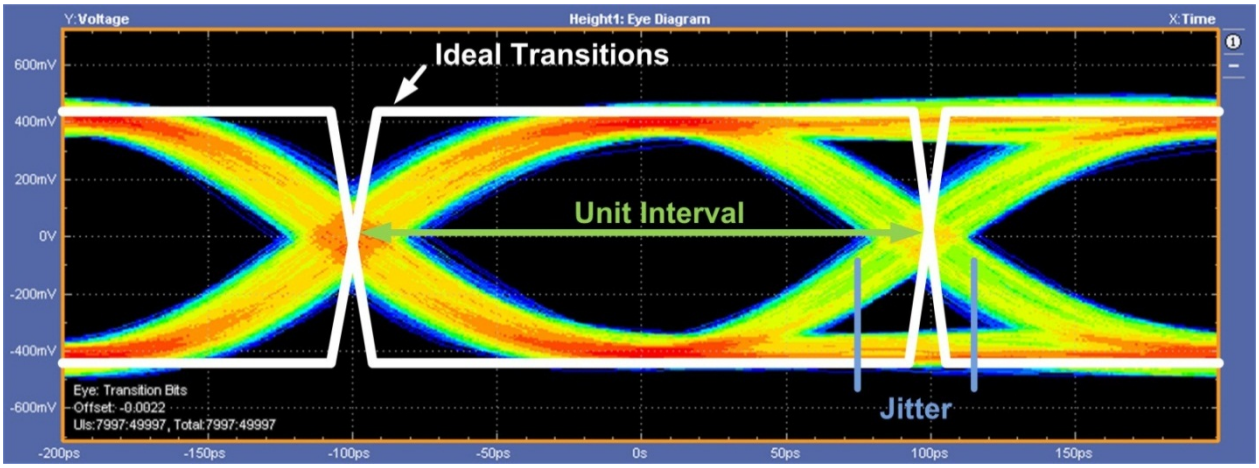


Figure 1. 5.0 Gbps Eye Diagram

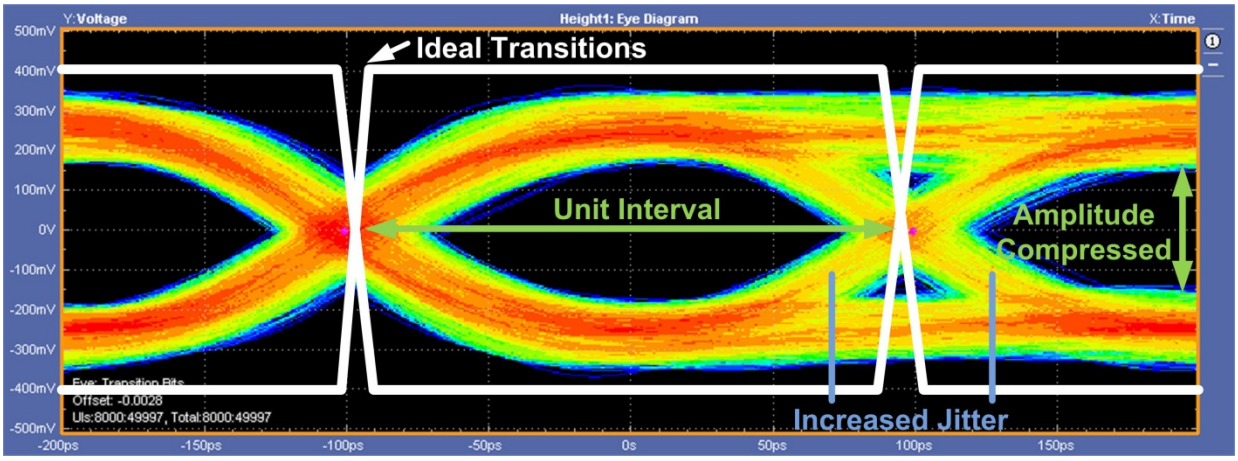


Figure 2. 5.0 Gbps Eye Diagram—Improper Termination

The eye diagram presented in Figure 3 presents another case of a nonideal transmission of data. In this case, an impedance discontinuity is presented at a point midway between the transmitter and the receiver (in this case an oscilloscope). As can be seen by the degraded performance in the plot, the eye opening is closing, meaning that the area inside the transition points is getting smaller. The rising edges and falling edges of the data severely degraded due to the reflections of the impedance discontinuity on the transmission line. The impedance discontinuity also contributes to an increase in the amount of jitter seen at the data transition points. Once the eye closes beyond the limits of the receiver's capability to decode the data stream, the data link will be lost. In the case of Figure 3, it is likely that many receivers would be unable to decode the data stream.

THE BATHTUB PLOT

In addition to the eye diagram, the bathtub plot also provides useful insight into the quality of the serial data transmission on a JESD204B data link. The bathtub plot is a measurement of the BER (bit error rate) as a function of the sampling point as it moves across the eye diagram in time. The bathtub plot is generated by moving the sampling point across the eye diagram and measuring the resultant BER at each point. As Figure 4 illustrates, the closer the sampling point is to the center of the eye, the BER decreases. As the sampling point moves closer to the transition points of the eye diagram, the BER increases. The distance between the two slopes of the bathtub plot at a given BER gives the eye opening at the specified BER (10^{-12} in this case).

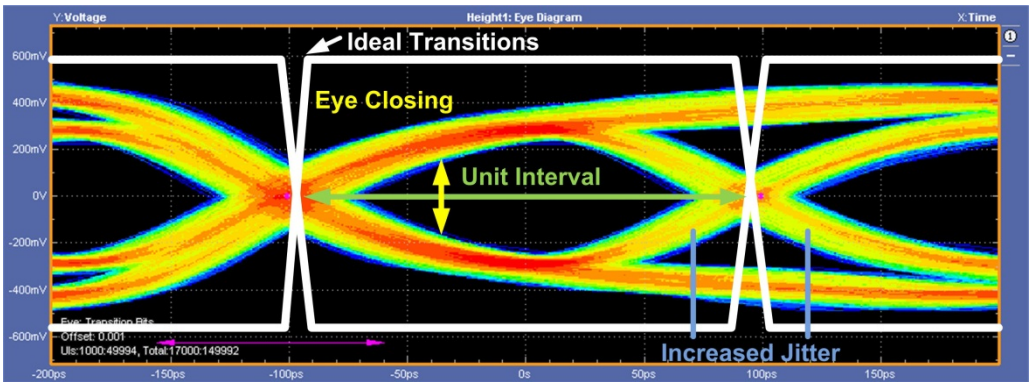


Figure 3. 5.0 Gbps Eye Diagram—Impedance Discontinuity

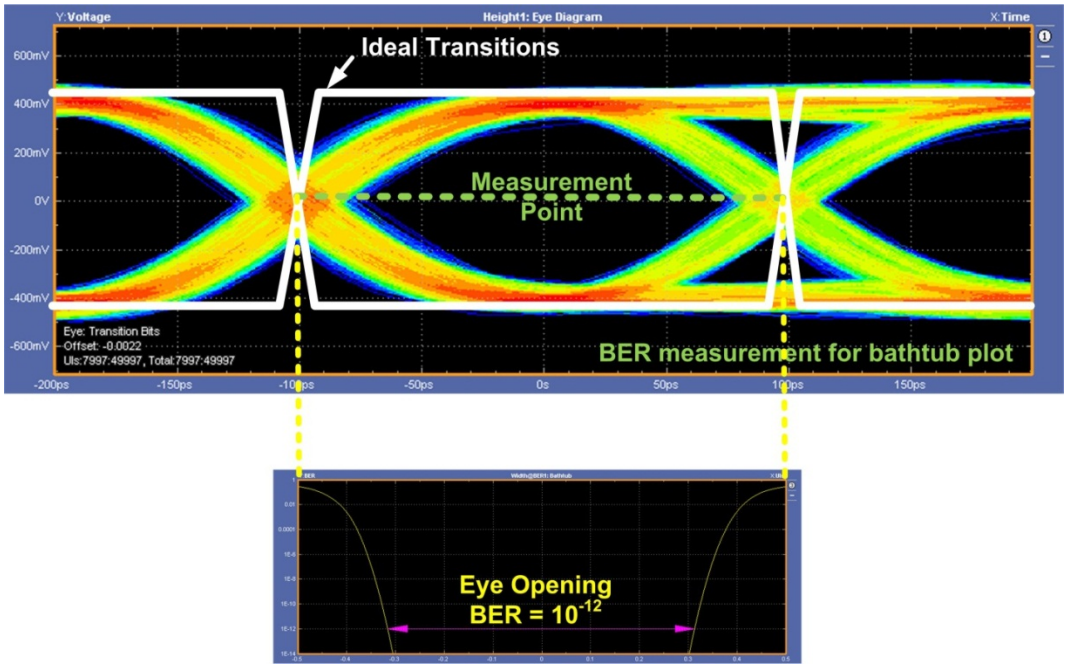


Figure 4. 5.0 Gbps Eye Diagram—Bathtub Plot Measurement

The bathtub plot also provides information on the jitter (Tj) components present in the signal. As Figure 5 shows, when the measurement point is at or near the transition points, it is relatively flat and the main jitter component is deterministic jitter. As with the eye diagram measurements, the bathtub plots are from measurements on a JESD204B 5.0 Gbps transmitter measured at the receiver after passing through a connecter and approximately 20 cm of transmission line. As the measurement point moves closer to the middle of the eye opening, the primary jitter mechanism is random jitter. Random jitter is the result of a large number of processes that are typically small in magnitude. Typical sources would include thermal noise, variations in trace width, shot noise, etc. The PDF (probability density function) of random jitter usually follows a Gaussian distribution. On the other hand, deterministic jitter results from a small number of processes that may have large magnitudes and may not be independent. The PDF of deterministic jitter is bounded and has a well-defined peak-to-peak value. It can have varying shapes and is typically not Gaussian.

An expanded view of the bathtub plot discussed in Figure 4 is given in Figure 6 below. This represents an eye opening of approximately 0.6 UI (unit interval) at the receiver for a 5.0 Gbps serial data transmission with a BER of 10^{-12}. It is important to note that the bathtub plot such as the one in Figure 6 is an extrapolated measurement. The oscilloscope used to capture the data takes a set of measurements and extrapolates the bathtub plot. If one were to use a BERT (bit error rate tester) and acquire enough measurements to build the bathtub plot, it could take hours or even days, even with the high speed operation of today's measurement equipment.

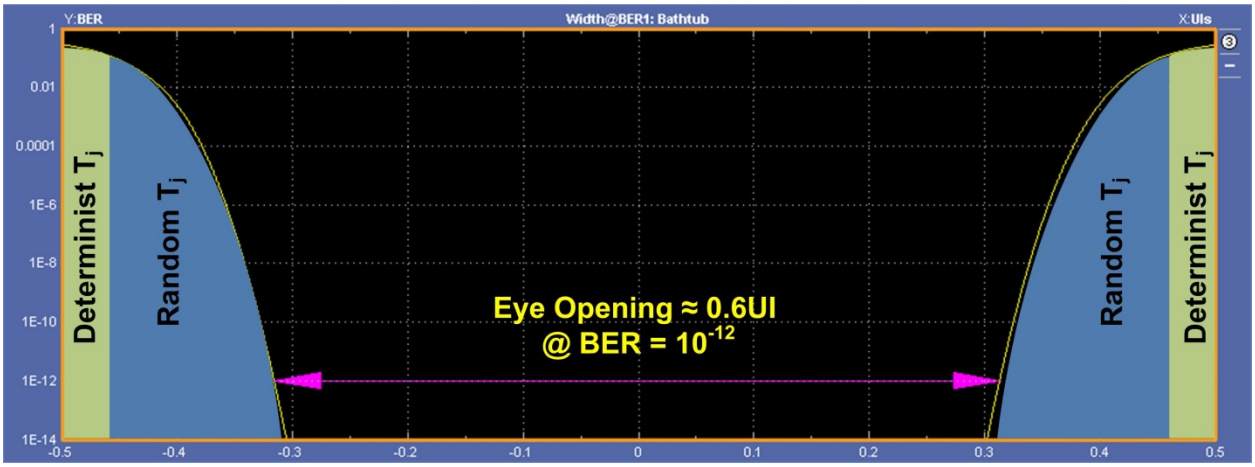


Figure 5. Bathtub Plot—Jitter Components

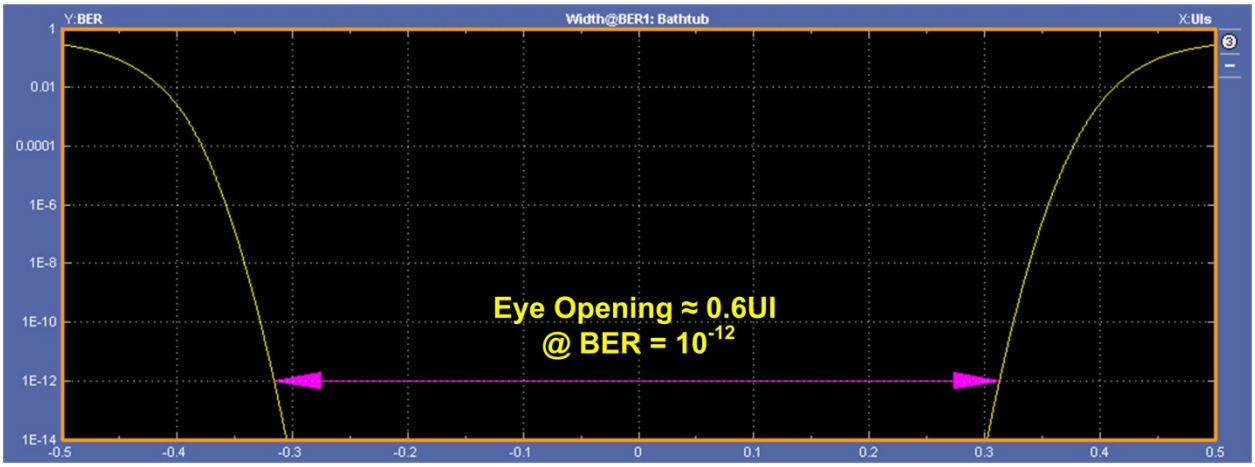


Figure 6. 5.0 Gbps Bathtub Plot

Just as shown in the eye diagram, an improper termination or impedance discontinuity in the system can be seen in the bathtub plot. In contrast to the bathtub plot in Figure 6, the bathtub plots in Figure 7 and Figure 8 exhibit much shallower slopes on each side. The eye opening for a BER of 10^{-12} is only 0.5 UI in both cases which is more than 10% less than the 0.6 UI for the good condition. The improper termination and impedance discontinuity contribute a large amount of random jitter to the system. This is evidenced by the decreasing slope on each side of the bathtub plot along with the decreased eye opening at a BER of 10^{-12}. There is also a small increase in the deterministic jitter as well. This is evidenced again by the decreasing slope near the edges of the bathtub plot.

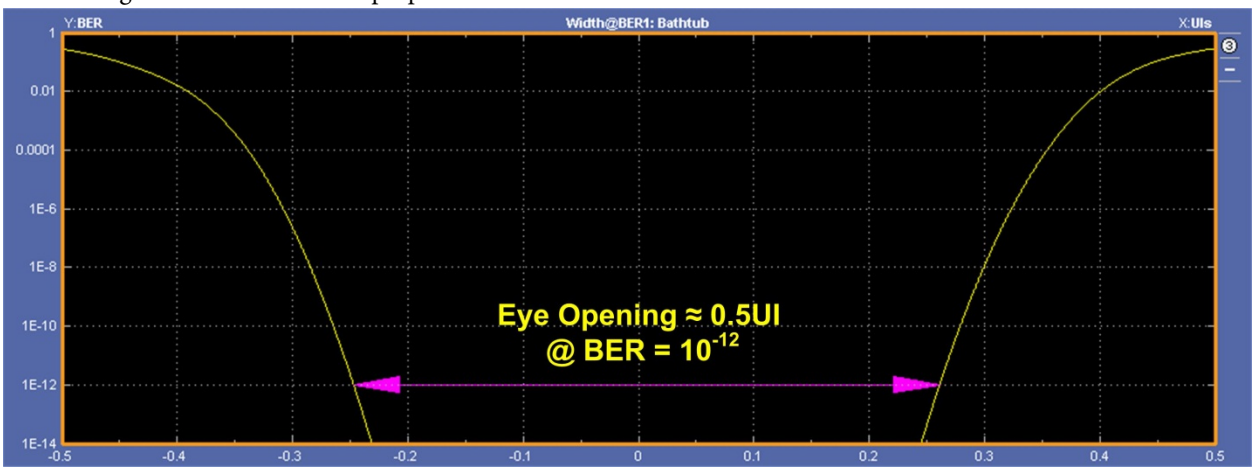


Figure 7. 5.0 Gbps Bathtub Plot—Improper Termination

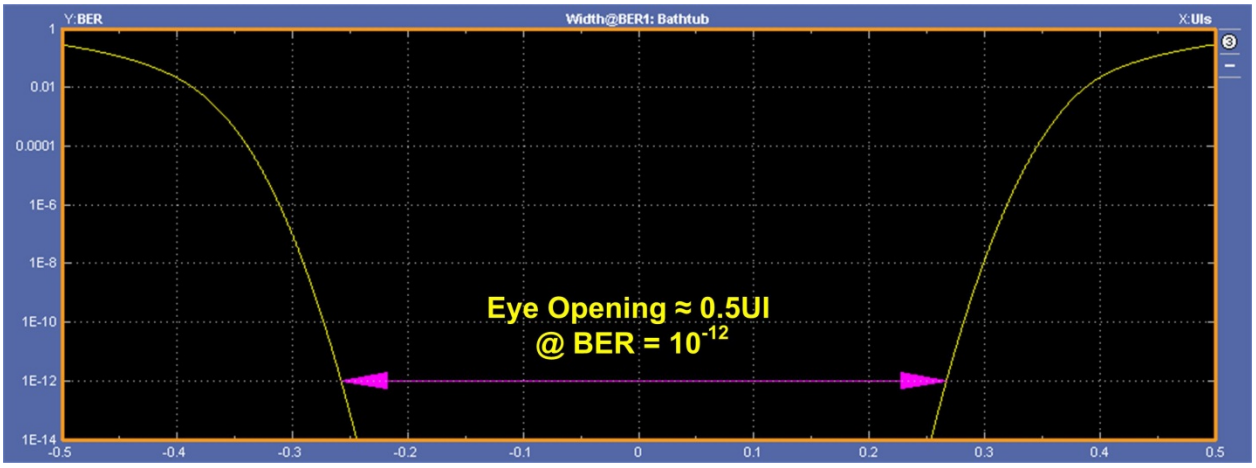


Figure 8. 5.0 Gbps Bathtub Plot—Impedance Discontinuity

THE HISTOGRAM PLOT

A third useful measurement is the histogram plot. This plot shows the distribution of the measured periods between transition points in the data transmission. As with the eye diagram and bathtub plot measurements, the histogram plots are from measurements on a JESD204B 5.0 Gbps transmitter measured at the receiver after passing through a connecter and approximately 20 cm of transmission line. Figure 9 shows a histogram for a relatively good performing system at 5.0 Gbps. The histogram shows a mostly Gaussian type distribution with periods measured between 185 ps and 210 ps. The expected period for a 5.0 Gbps signal should be 200 ps which means the distribution is spread about −7.5% to +5% around its expected value.

When an improper termination is introduced, as shown in Figure 10, the distribution becomes wider and now varies between 170 ps and 220 ps. This increases the percentage of variation from −15% to +10%, which is double that of the measurement shown in Figure 9. These plots show that mostly random jitter is present in the signal since they have a mostly Gaussian-like shape. However, the shape is not exactly Gaussian in nature which indicates there is at least a small amount of deterministic jitter also.

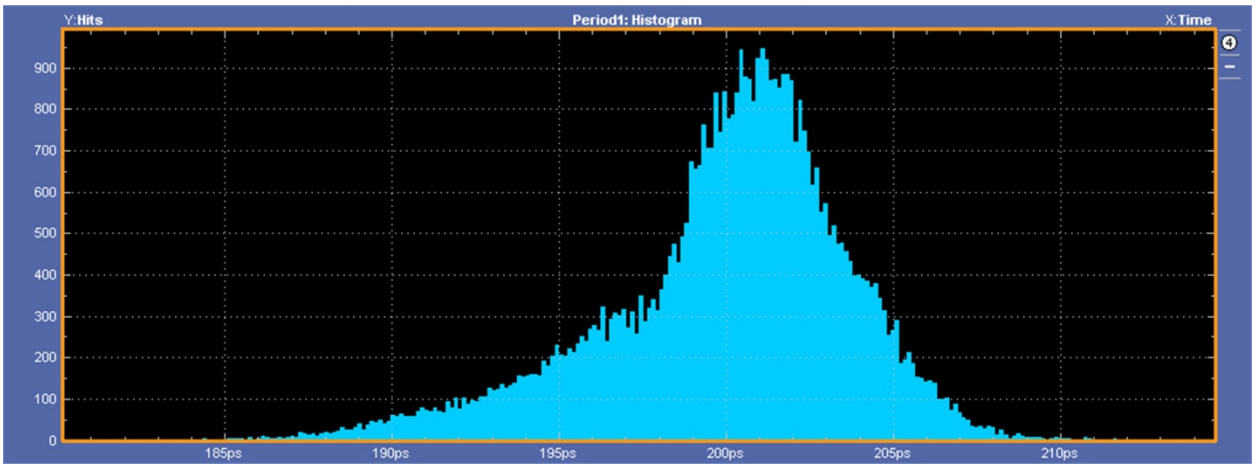


Figure 9. 5.0 Gbps Histogram Plot

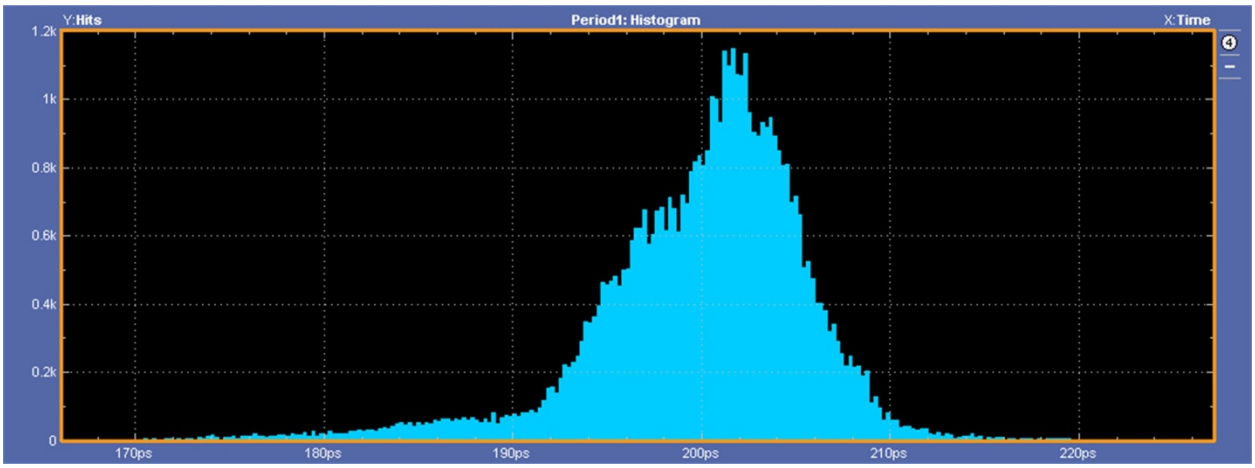


Figure 10. 5.0 Gbps Histogram Plot—Improper Termination

The histogram presented in Figure 11 indicates the results of having an impedance discontinuity along the transmission line. The shape of the distribution is not Gaussian-like at all and has developed a small secondary hump. The mean value of the measured period is also skewed. Unlike the plots in Figure 9 and Figure 10, the mean is no longer 200 ps and has shifted to about 204 ps. The more bimodal distribution indicates that there is more deterministic jitter in the system. This is due to the impedance discontinuity present on the transmission lines and the predictable impacts this has on the system. The range of values measured for the period is again increased, although not as much as in the case of improper termination. In this case, the range is from 175 ps up to 215 ps, which is a range of approximately −12.5% to +7.5% of the expected period. The range isn't as large, but again, the distribution is more bimodal in nature.

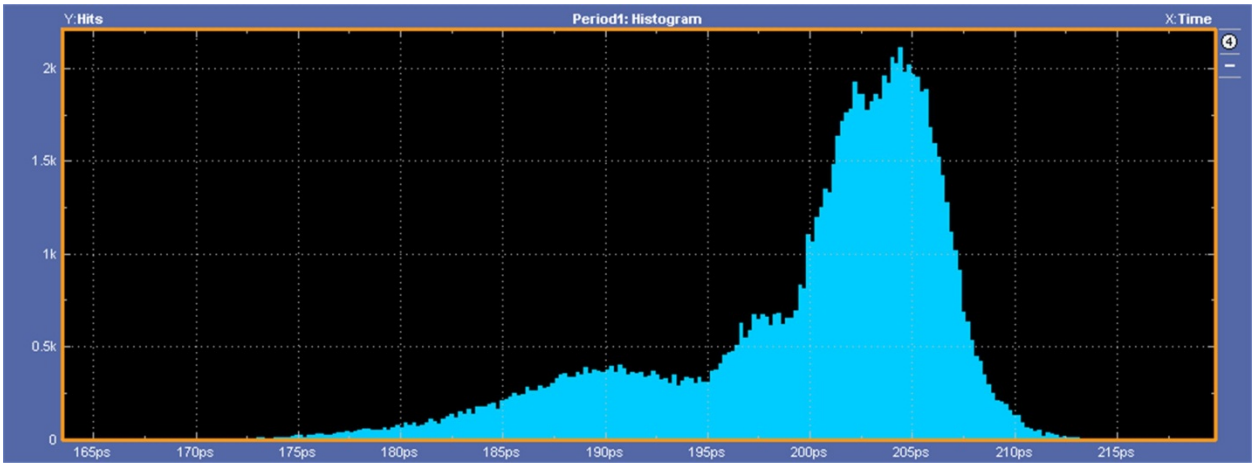


Figure 11. 5.0 Gbps Histogram Plot—Impedance Discontinuity

CONCLUSION

Several performance metrics can be used to evaluate the performance of the physical layer of a JESD204B transmitter. These include common-mode voltage, differential peak-to-peak voltage, differential impedance, differential output return loss, common-mode return loss, transmitter short circuit current, eye diagram mask, and jitter. Three key performance metrics have been discussed that are used to evaluate the quality of the transmitted signal. The eye diagram, bathtub plot, and histogram plot are three important performance metrics that are used to evaluate the quality of the JESD204B link. System issues such as improper terminations and impedance discontinuities have significant impact on the performance of the physical layer. These impacts are evidenced by the degraded performance shown in the eye diagrams, bathtub plots, and histogram plots. It is important to maintain good design practices to properly terminate the system and to avoid impedance discontinuities in the transmission media. These have appreciable negative effects on the data transmission and can result in a faulty data link between the JESD204B transmitter and receiver. Employing techniques to avoid these issues will help to ensure a properly working system.

ABOUT THE AUTHOR

Jonathan Harris is a product applications engineer in the High Speed Converter Group at Analog Devices in Greensboro, NC. He has over seven years of experience as an applications engineer, supporting products in the RF industry. Jonathan received his MSEE from Auburn University and his BSEE from UNC-Charlotte. In his spare time, he enjoys mobile audio, nitro R/C, college football, and spending time with his two children.

REFERENCES

JEDEC Standard JESD204B (July 2011). JEDEC Solid State Technology Association. www.jedec.org

Application Note 5989-5718EN. "Using Clock Jitter Analysis to Reduce BER in Serial Data Applications." Agilent Technologies, December 2006.

Application Note 5988-9109EN. "Measuring in Digital Systems." Agilent Technologies, January 2008.

RESOURCES

Share this article on  

One Technology Way • P.O. Box 9106 • Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 • Fax: 781.461.3113 • www.analog.com

TA11324-0-1/13

The ABCs of Interleaved ADCs

by Jonathan Harris, Applications Engineer, Analog Devices, Inc.

INTRODUCTION

Across many segments of the market today, interleaving ADCs offers several advantages in many applications. In communications infrastructure there is constantly a push for higher sample rate ADCs to allow for multiband, multicarrier radios, in addition to wider bandwidth requirements for linearization techniques like DPD (digital predistortion). In military and aerospace, higher sample rate ADCs allow for multipurpose systems that can be used for communications, electronic surveillance, and radar just to name a few. In yet another segment, industrial instrumentation, the need is always increasing for higher sample rate ADCs so that higher speed signals can be measured adequately and accurately.

It is first important to understand exactly what interleaving ADCs is about. To understand interleaving, it is good to look at what is actually happening and how it is being implemented. With a basic understanding, the benefits of interleaving can then be discussed. Of course, as many know, there is no such thing as a free lunch, so the challenges of interleaving need to be evaluated and assessed.

ABOUT INTERLEAVING

When ADCs are interleaved, two or more ADCs with a defined clocking relationship are used to simultaneously sample an input signal and produce a combined output signal that results in a sampling bandwidth at some multiple of the individual ADCs. Utilizing ***m*** number of ADCs allows for the effective sample rate to be increased by a factor of ***m***. For the sake of simplicity and ease of understanding, we'll focus on the case of two ADCs. In this case, if two ADCs with each having a sample rate of f_S are interleaved, the resultant sample rate is simply $2f_S$. These two ADCs must have a clock phase relationship for the interleaving to work properly. The clock phase relationship is governed by Equation 1, where ***n*** is the specific ADC and ***m*** is the total number of ADCs.

$$\emptyset_n = 2\pi\left(\frac{n-1}{m}\right) \quad (1)$$

As an example, two ADCs each, with a sample rate of 100 MSPS, are interleaved to achieve a sample rate of 200 MSPS. In this case, Equation 1 can be used to derive the clock phase relationship of the two ADCs and is given by Equation 2 and Equation 3.

$$\emptyset_1 = 2\pi\left(\frac{1-1}{2}\right) = 0\ radians = 0^o \quad (2)$$

$$\emptyset_2 = 2\pi\left(\frac{2-1}{2}\right) = \pi\ radians = 180^o \quad (3)$$

Now that the clock phase relationship is known, the construction of samples can be examined. Figure 1 gives a visual representation of the clock phase relationship and the sample construction of two 100 MSPS interleaved ADCs. Notice the 180° clock phase relationship and how the samples are interleaved. The input waveform is alternatively sampled by the two ADCs. In this case, the interleaving is implemented by using a 200 MHz clock input that is divided by a factor of two and the required phases of the clock to each ADC.

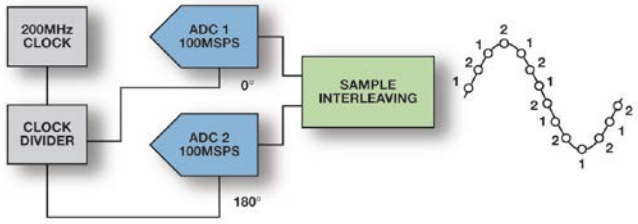


Figure 1. Two Interleaved 100 MSPS ADCs—Basic Diagram

Another representation of this concept is illustrated in Figure 2. By interleaving these two 100 MSPS ADCs, the sample rate is increased to 200 MSPS. This extends each Nyquist zone from 50 MHz to 100 MHz, doubling the available bandwidth in which to operate. The increased operational bandwidth brings many advantages to applications across many market segments. Radio systems can increase the number of supported bands; radar systems can improve spatial resolution, and measurement equipment can achieve greater analog input bandwidth.

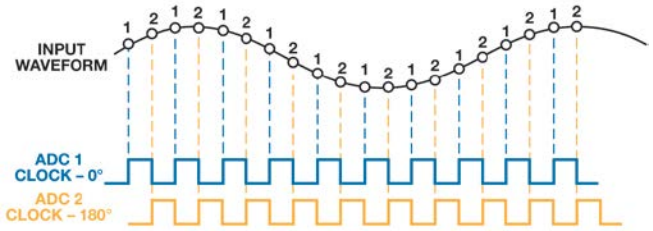


Figure 2. Two Interleaved 100 MSPS ADCs—Clocking and Samples

BENEFITS OF INTERLEAVING

The benefits of interleaving span across multiple segments of the market. The most desired benefit of interleaving is the increased bandwidth made possible by the wider Nyquist zone of the interleaved ADCs. Once again, taking the example of two 100 MSPS ADCs interleaved to create a sample rate of 200 MSPS, Figure 3 gives a representation of the much wider bandwidth allowed by interleaving the two ADCs. This creates advantages for many different applications. As cellular standards increase channel bandwidth and the number of operating bands, there are increased demands on the available bandwidth in the ADC. In addition, in military applications, the requirements for better spatial recognition, as well as increased channel bandwidths in backend communications require higher bandwidths from the ADC. Due to the increased demands for bandwidth in these areas, there is a need created to measure these signals accurately. Therefore, measurement equipment has increased needs for higher bandwidths in order to properly acquire and measure these signals that have higher bandwidth. The system requirements in many designs inherently stay ahead of commercial ADC technology. Interleaving allows for some of this gap to be closed.

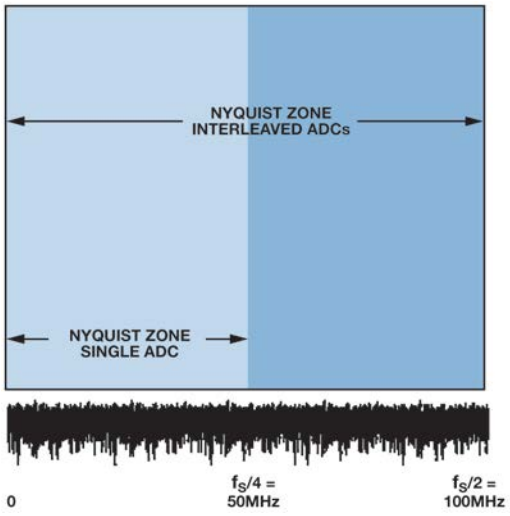


Figure 3. Two Interleaved ADCs—Nyquist Zone

The increased sample rate provides more bandwidth for these applications but also allows for easier frequency planning and reduction in the complexity and cost of the anti-aliasing filter that is typically used at the ADC inputs. With all these great benefits, one has to wonder what the price is to pay. As with most things, there is no such thing as a free lunch. Interleaved ADCs offer increased bandwidth and other nice benefits, but there are some challenges that arise when dealing with interleaved ADCs.

CHALLENGES WITH INTERLEAVING

There are some challenges and things to look out for when interleaving ADCs. There are spurs that appear in the output spectrum that result from the imperfections associated with interleaving ADCs. These imperfections are basically mismatches between the two ADCs that are being interleaved. There are four basic mismatches that result in spurs in the output spectrum. These are offset mismatch, gain mismatch, timing mismatch, and bandwidth mismatch.

The easiest of these to understand is probably the offset mismatch between the two ADCs. Each ADC will have an associated dc offset value. When the two ADCs are interleaved and samples are acquired alternatively back and forth between the two ADCs, the dc offset of each successive sample is changing. Figure 4 gives an example of how each ADC has its own dc offset and how the interleaved output will effectively switch back and forth between these two dc offset values. The output switches between these offset values at a rate of $f_S/2$ which will result in a spur in the output spectrum located at $f_S/2$. Since the mismatch itself does not have a frequency component and is only at dc, the frequency of the spur that appears in the output spectrum only depends on the sampling frequency and will always appear at a frequency of $f_S/2$. The magnitude of the spur is dependent upon the magnitude of the offset mismatch between the ADCs. The greater the mismatch, the larger the spur will be. In order to minimize the spur caused by the offset mismatch, it is not necessary to completely null the dc offset in each ADC. Doing this would filter out any DC content in the signal and would not work for systems using a ZIF (zero IF) architecture where the signal content is real and complex and includes data at DC. Instead, a more appropriate technique would be to match the offset of one of the ADCs to the other ADC. The offset of one ADC is chosen as the reference, and the offset of the other ADC is set to match that value as closely as possible. The better matched the offset values are, the lower the resulting spur is at $f_S/2$.

The second mismatch to look at when interleaving is the gain mismatch between the ADCs. Figure 5 gives a representation of the gain mismatch between two interleaved converters. In this case, there is a frequency component to the mismatch. In order to observe this mismatch, there has to be a signal applied to the ADCs. In the case of the offset mismatch, no signal is necessary to see the inherent dc offset of the two ADCs. In the case of the gain mismatch, there is no way to see the gain mismatch unless a signal is present and the gain mismatch can be measured. The gain mismatch will result in a spur in the output spectrum that is related to the input frequency, as well as the sampling rate, and will appear at $f_S/2 \pm f_{IN}$. In order to minimize the spur caused by

the gain mismatch, a similar strategy as what is used for the offset mismatch is employed. The gain of one of the ADCs is chosen as the reference, and the gain of the other ADC is set to match that gain value as closely as possible. The better the gain values of each ADC are matched to each other, the less the resulting spur will be in the output spectrum.

Next, we must examine the timing mismatch between the two ADCs. The timing mismatch has two components, group delay in the analog section of the ADC and clock skew. The analog circuitry within the ADC has an associated group delay and the value can be different between the two ADCs. In addition, there is clock skew that has an aperture uncertainty component in each of the ADCs and has a component related to the accuracy of the clock phases that are input to each converter. Figure 6 gives a visual representation of the mechanism and effects of the timing mismatches in the ADCs. Similar to the gain mismatch spur, the timing mismatch spur is also a function of the input frequency and the sample rate and appears at $f_S/2 \pm f_{IN}$. In order to minimize the resulting spur, the group delay through the analog section of each converter needs to be properly matched with good circuit design techniques. In addition, the clock path designs need to be closely matched to minimize aperture uncertainty differences. And lastly, the clock phase relationships need to be precisely controlled such that the two input clocks are as close to 180° apart as possible. As with the other mismatches, the goal is to attempt to minimize the mechanisms that cause the timing mismatch.

The last mismatch to look at is probably the most difficult to comprehend and handle; it is the bandwidth mismatch. As shown in Figure 7, the bandwidth mismatch has a gain and a phase/frequency component. This makes bandwidth mismatch more difficult because it contains components from two of the other mismatch parameters. In the bandwidth mismatch, however, we see different gain values at different frequencies. In addition, the bandwidth has a timing component which causes signals at different frequencies to have different delays through each converter. The best way to minimize the bandwidth mismatch is to have very good circuit design and layout practices that work to minimize the bandwidth mismatches between the ADCs. The better matched each ADC is, the less the resulting spur will be. Just as the gain and timing mismatches caused spurs in the output spectrum at $f_S/2 \pm f_{IN}$, the bandwidth mismatch also results in a spur at the same frequency.

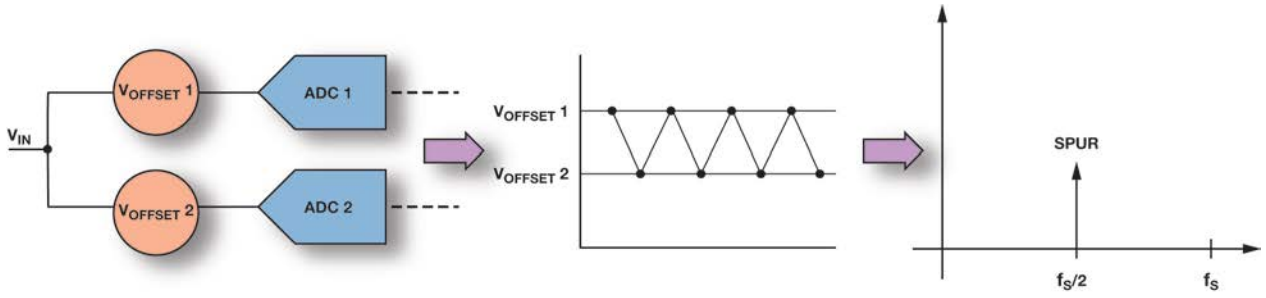


Figure 4. Offset Mismatch

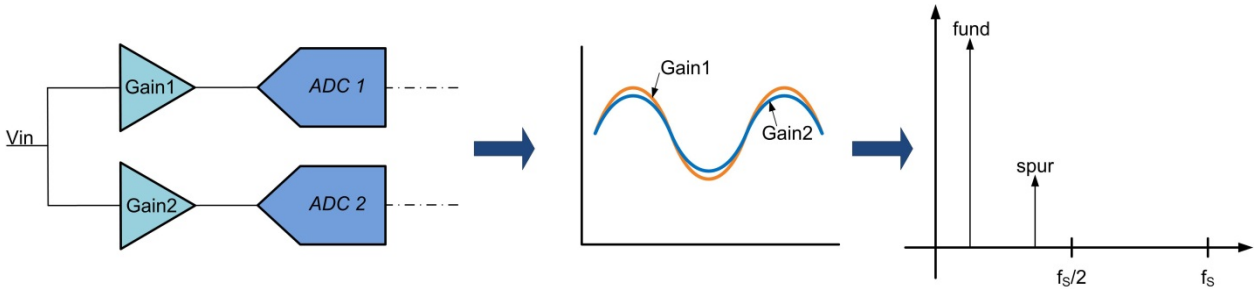


Figure 5. Gain Mismatch

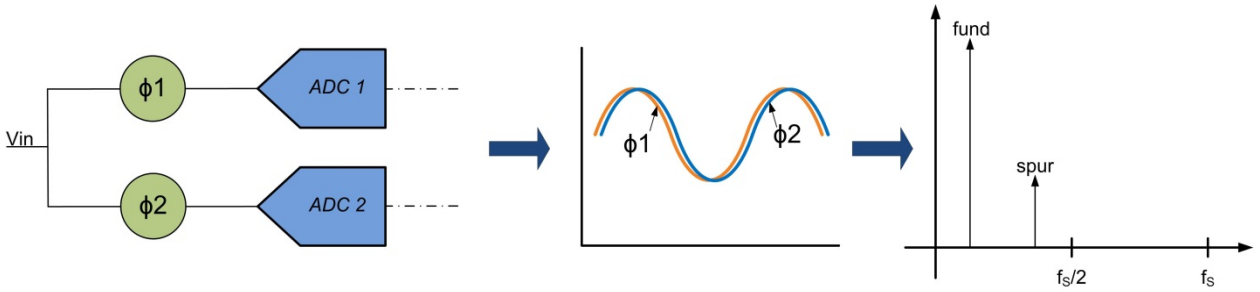


Figure 6. Timing Mismatch

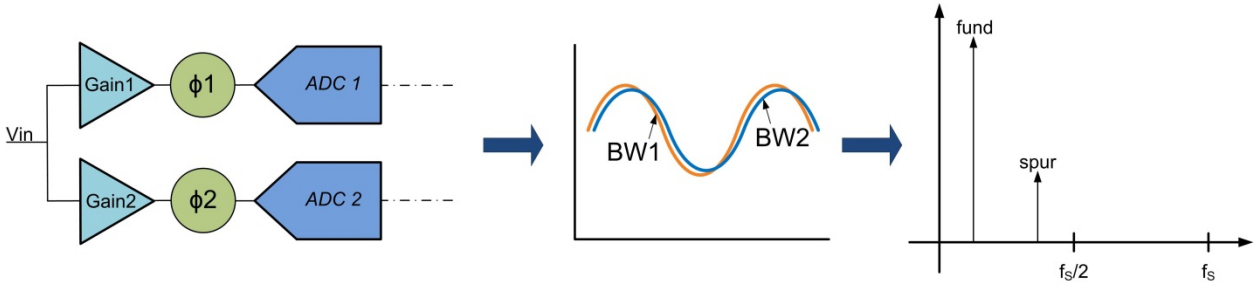


Figure 7. Bandwidth Mismatch

Now that we've discussed four different mismatches that cause issues when interleaving ADCs, it is apparent that a commonality has emerged. Three of the four mismatches produce a spur in the output spectrum at $f_S/2 \pm f_{IN}$. The offset mismatch spur can be easily identified since it alone resides at $f_S/2$ and can be compensated fairly easily. The gain, timing, and bandwidth mismatches all produce a spur at $f_S/2 \pm f_{IN}$ in the output spectrum so the question is how to identify the contribution of each. Figure 8 gives a quick visual guide to the process of identifying the sources of the spurs from the different mismatches of interleaved ADCs.

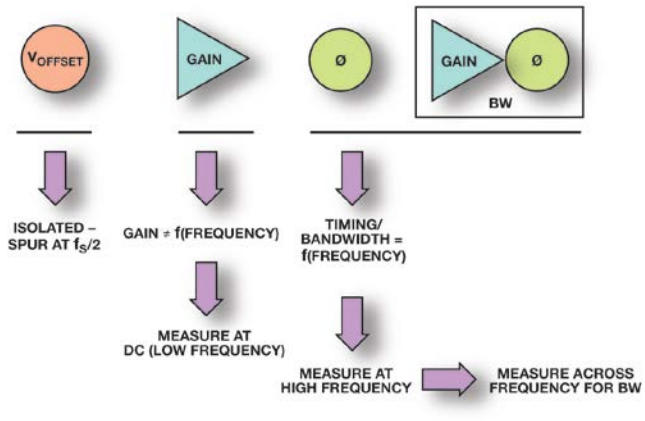


Figure 8. Interrelated Nature of Interleaving Mismatches

If looking purely at gain mismatch alone, it is a low frequency, or dc, type of mismatch. The gain component of the bandwidth mismatch can be separated from the gain mismatch by performing a gain measurement at low frequency near dc and then performing gain measurements at higher frequencies. The gain mismatch is not a function of frequency like the gain component of the bandwidth mismatch. A similar approach is used for the timing mismatch. A measurement is performed at low frequency near dc and then subsequent measurements are performed at higher frequencies to separate the timing component of bandwidth mismatch from the timing mismatch.

CONCLUSION

The newest communication system designs, cutting edge radar technologies, and ultrahigh bandwidth measurement equipment seem to constantly outpace the available ADC technology. These requirements push both users and manufacturers of ADCs to develop methods to keep pace with these demands. Interleaving ADCs allows for greater bandwidths to be achieved at a faster pace than the traditional path of increasing the conversion rate of a typical ADC. By taking two or more ADCs and interleaving them together, the available bandwidth is increased, and system design requirements can be met at a faster pace. Interleaving ADCs does not come for free, however, and mismatches between the ADCs cannot be ignored. Even though the mismatches do exist, knowing about them and how to appropriately deal with them can enable designers to use these interleaved ADCs more intelligently and meet the ever increasing demands of their latest system designs.

REFERENCES

Had, Jim, Mark Looney, and Rob Reeder. "Pushing the State of the Art with Mulitchannel A/D Converters." *Analog Dialogue*. Vol. 39, No. 5, May 2005.

RESOURCES

Share this article on  

One Technology Way • P.O. Box 9106 • Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 • Fax: 781.461.3113 • www.analog.com

TA11329-0-1/13

New, Faster JESD204B Standard for High Speed Data Converters Comes with Verification Challenges

by Frank Farrelly, Product Engineering Manager, Analog Devices, Inc., and Chris Loberg, Senior Technical Marketing Manager, Tektronix

IDEA IN BRIEF

JESD204B is a new 12.5 Gb/s serial interface standard for high speed, high resolution data converters. Already, devices from converter manufacturers are beginning to make their way into the market, and it is expected that the number of JESD204B-enabled products will increase tremendously in the near future. The primary value of the JESD204B interface is a reliable increase in the data transfer bandwidth between a converter and a logic device (such as an FPGA or ASIC).

As with any new interface, JESD204B brings new challenges. For system developers, the challenges are how to best implement JESD204B from a PCB design standpoint and how to debug a system if something isn't initially working right. For component manufacturers, challenges involve testing new JESD204B devices. Testing not only ensures that specifications are being met in a relatively ideal environment, but it also ensures successful JESD204B operation in end system environments.

This article discusses the JESD204B specification, reviews the tesets needed to validate JESD204B devices, and outline methods used to replicate end system environments.

JESD204B—A NATURAL EVOLUTION FOR DATA CONVERTERS

Data converters (digital-to-analog and analog-to-digital) are used in many applications ranging from audio and music to test instrumentation. The world of data converters is evolving. As the bit depth and sample rate go up, it is becoming more and more difficult to get data in and out. A decade or two ago, with sample rates for high speed converters limited to 100 MSPS and below, using TTL or CMOS parallel data busses was sufficient. For example, a 12-bit converter with 12 pins dedicated to the data could be implemented with reasonable setup and hold times with respect to the clock.

As speeds increased above 100 MSPS, setup and hold times for single-ended signals could no longer be maintained. To boost speeds, high speed converters moved to differential signaling but at the cost of increased pin counts. For example, a 12-bit converter now would need 24 pins dedicated to data. To address the pin count issue, serial data interfaces were adopted. A converter data interface with 6× serialization now allows that same 12-bit converter to transfer the data with just two differential I/Os (only four pins). Fast forwarding to today, data converters are now being developed using the JESD204B specification for the data interface.

The JEDEC standards organization has published two versions of the JESD204 high speed serial digital interface specification. The first version, the JESD204 2006 specification, brought the advantages of SerDes-based high speed serial interfaces to data converters with a 3.125 Gbps maximum speed rating. It was revised in 2008, (JESD204A 2008 specification) and added important enhancements including support for multiple data lanes and lane synchronization. The second version of the specification, JESD204B, was developed by an international JEDEC JC-16 task group (Project 150.01), comprised of about 65 members from 25 companies. It provided a number of major enhancements including a higher maximum lane rate, support for deterministic latency through the interface, and support for harmonic frame clocking.

LACK OF AN OFFICIAL COMPLIANCE TEST SPECIFICATION

Unlike many other high speed serial interface standards, the JESD204B standard does not include an official compliance test specification. A test specification is doubly valuable because it lists the tests which must be performed to ensure compatibility, as well as the procedures for doing those tests. Having consistent procedures used by different manufacturers help ensure a common understanding of the specification and eliminate differences in assumptions. The lack of an official compliance test specification does not mean that all is lost. All of the information needed to develop a set of tests and procedures can be found in the JESD204B specification and the specifications it refers to. It is left up to the individual chip manufacturers and system developers to pull together that information.

PHYSICAL LAYER TESTING

Physical layer, or PHY, tests are related to the individual data lane driver and receiver circuitry: in other words, the analog tests of a link. They do not include digital functionality or procedural tests. Working toward the goal of developing a thorough list of PHY tests, a list of recommended SerDes PHY tests can be obtained from the OIF-CEI-02.0 specification, Section 1.7. The JESD204B specification closely follows those recommendations but does include a few modifications. For example, JESD204B does not specify random jitter as a standalone test item, rather choosing to include it under total jitter. Also, JESD204B specifies JSPAT, JTSPAT, and modified RPAT as recommended test patterns, whereas the OIF-CEI-02.0 specifies using the PRBS31 pattern.

Above and beyond the required PHY tests, there are additional PHY tests that could be performed which are not listed in the OIF-CEI-02.0 specification or in the PHY section of the JESD204B specification. One can look to other SerDes compliance test specifications for examples and find tests such as intrapair skew (for a Tx) and intrapair skew tolerance (for an Rx). In bringing these up, it is not the intention to recommend that these tests be added to the JESD204B specification. Additional PHY tests are not required to ensure JESD204B compatibility. The intention is to note that if a particular PHY test is failing, other PHY tests can be used to help gain insight as to why.

Once the list of tests is set, limits for those tests can be obtained from the JESD204B specification. Just keep in mind that there are three sets of limits: LV-OIF-11G-SR, LV-OIF-6G-SR, and LV-OIF-SxI5. A particular JESD204B device may support more than one set of limits. In that case, the component should be tested against all of the sets of limits that are supported.

One point of potential confusion with JESD204B PHY testing is jitter terminology. The JESD204B and OIF-CEI-02.0 specifications use different terminology from what the test equipment vendors use. The typical jitter map is shown in Figure 1. Test equipment makers base their terminology on the industry standard dual Dirac jitter model. This difference in terminology is a point of potential problems in test procedures, as jitter is quite a tricky topic. Table 1 shows our translation of the jitter terminology (the JESD204B specification uses different terminology for jitter from that used by test equipment vendors).

Table 1. Jitter Terms Translation

JESD204B Jitter Term	JESD204B Jitter Name	Test Equipment Jitter Translation
T_UBHPJ	Transmit uncorrelated bounded high probability jitter	BUJ (PJ and NPJ)
T_DCD	Transmit duty cycle distortion	DCD
T_TJ	Transmit total jitter	TJ
R_SJ-HF	Receive sinusoidal jitter, high frequency	PJ > 1/1667 × BR
R_SJ-MAX	Receive sinusoidal jitter, maximum	PJ < 1/166,700 × BR
	Receive bounded high probability jitter—correlated	DDJ
R_BHPJ	Receive bounded high probability jitter—uncorrelated	NPJ
R_TJ	Receive total jitter	TJ

Figure 1. Typical Jitter Map, Including Identification of Bounded Uncorrelated Jitter (BUJ)

Another point of potential confusion with JESD204B PHY testing is the eye mask for data rates above 11.1 Gbps. The JESD204B specification says that for data rates greater than 11.1 Gbps to use a normalized bit time of 11.1 Gbps. So, if running at 12.5 Gbps (with an 80 ps bit period), it says to use the bit period for 11.1 Gbps (90.9 ps). The issue at hand here is that eye masks can be built by starting either at the edge of the UI or from the center of the UI, and the JESD204B does not clearly state which reference point to start from. If the reference point is the center of the UI, then the eye mask is bigger than normal at 12.5 Gbps, making it harder for a Tx to pass but easier for an Rx to work. If the reference point is the edge of the UI, then the eye mask is smaller than normal at 12.5 Gbps, making it easier for a Tx to pass but hard for an Rx to work. Ultimately, until this question is resolved, it is recommended to test against each of the two mask options in order to ensure compatibility.

TIMING TESTING

Coming up with a thorough list of timing tests for JESD204B is not an easy task. There are at least dozen timing diagrams throughout the specification, and it's not immediately apparent which apply to the Tx, the channel, or the Rx. Also, some are only applicable to a particular subclass (0, 1, or 2). An official compliance test specification would be especially helpful here if it were to simply consolidate the timing specifications into a single table. Once time is taken to methodically go through the timing specifications, there is no confusion about them.

One nice thing about timing for system developers is that specifying timing for a JESD204B component turns out to be easier than is immediately apparent from the specification. For Subclass 0 and 2, only Device Clock-to-SYNC~ timing must be specified. For Subclass 1, only Device Clock-to-SYSREF timing must be specified.

PROTOCOL TESTING

As with the PHY tests, there is no official list of JESD204B protocol tests. Therefore, it is left to each user to scour through the specification and compile a list of functions to test. This section lists many of the suggested protocol tests and briefly describes them.

One category of protocol tests are the test sequences. For PHY testing, JESD204B transmitters must be able to output JSPAT and modified RPAT patterns. From a protocol standpoint, there's a need to validate that those patterns are correct. The same is true with JESD204B receivers and the JTSPAT pattern. Optionally, if they support PRBS patterns, those need to be validated as well. Next, are the short and long transport layer patterns. These are included to help system developers debug their systems by proving that the

link is working correctly through the transport layer. From a component manufacturer standpoint, those transport layer patterns have to be validated for every mode of operation that the device supports, which, considering the number of link configuration variables, ends up being a lot of cases.

One question that comes up regarding protocol testing is how to do it at 12.5 Gbps. One recommended solution is to use a high speed oscilloscope with a serial data decoder. Many higher end oscilloscopes are now equipped with a dedicated trigger chip for triggering on 8b/10b data such as that used in JESD204B. Figure 3 shows serial decode of a JESD204B data lane at 6 Gb/s at the beginning of the initial lane alignment sequence (ILAS) sequence.

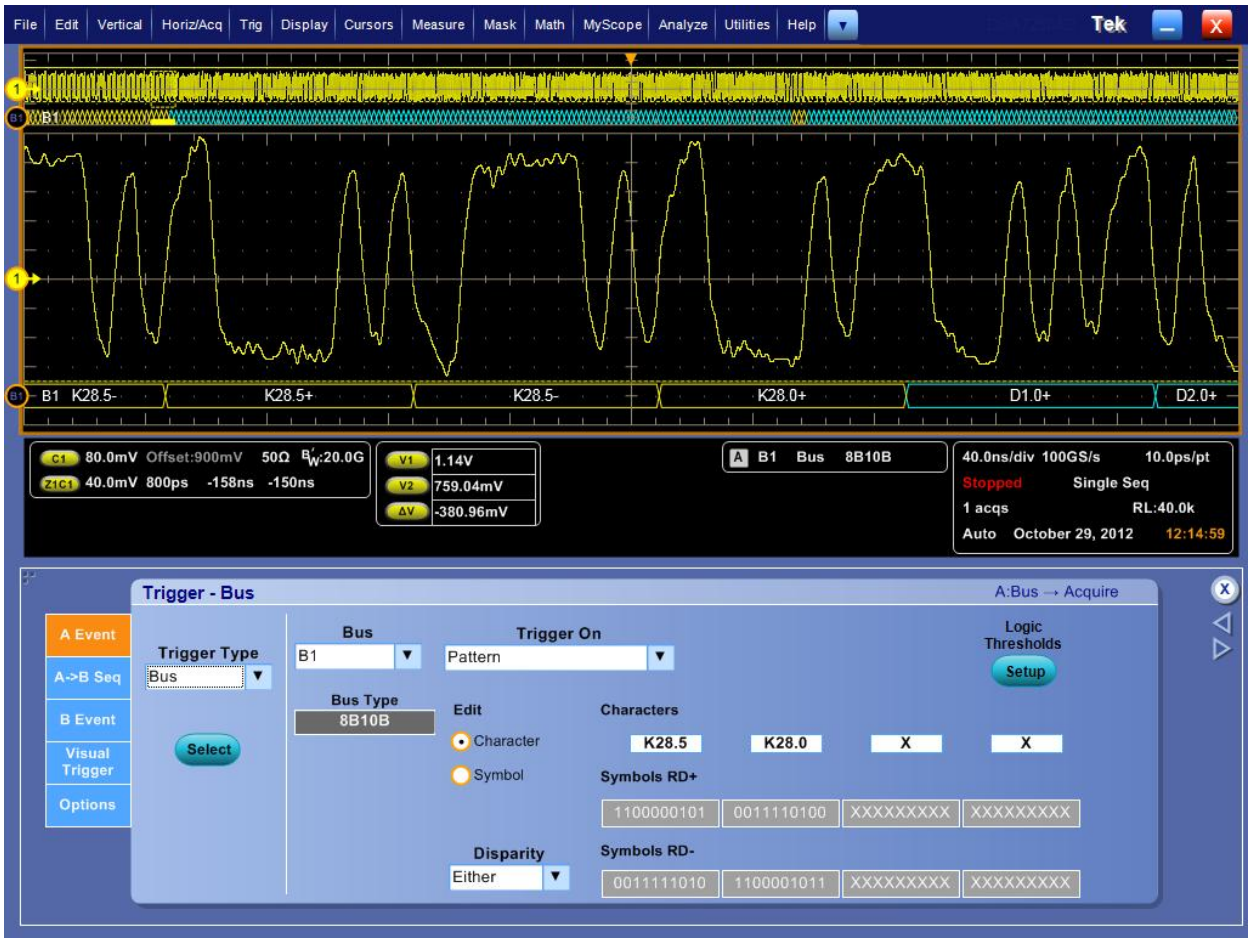


Figure 2. Serial Decode of a JESD204B Data Lane at 6 Gbps Showing the Beginning of the ILAS Sequence

Another group of protocol tests can be built around the ILAS. The ILAS as a whole is fairly complex, so breaking it down into its individual components can make protocol testing more meaningful. The following are some examples of tests that can be measured on a transmitter to validate its operation. Is the multiframe length correct? Does each multiframe start with an /R/ control code and end with an /A/ control code? Is the /Q/ control code in the right location? Is the link configuration data correct and in the right location? The ILAS contains data; is that correct? How many multiframes does the ILAS last? Is the ILAS the same on all lanes? Clearly, there is a lot of potential for protocol testing around the ILAS sequence.

JESD204B does not have a lot of handshaking, but what it does have can be tested. Depending on the subclass, a number of tests can be performed. Since the SYNC~ signal can be used for initial handshaking, error reporting, and link reinitialization, do the Tx and Rx components do their part accordingly? Does the Rx assert SYNC~ starting at the right time and for the right duration? Does the Tx react correctly based on the duration of SYNC~ assertion? Since the data sent over the link also plays a part in the handshaking (i.e., the ILAS), is it correct for its content and with respect to SYNC~ timing?

Next, there are a number of smaller digital functions that need to be tested as part of protocol, including scrambling, 8b/10b encoding/decoding, skew and skew tolerance, control bits, tail bits, SYNC~ signal combining, frame alignment monitoring, and correction. All of these functions need to be validated.

Lastly, there is the category of protocol tests called error handling. The specification includes a minimum set of errors that must be detected and reported: disparity errors, not-in-table errors, unexpected control character errors, and code group synchronization errors. But, there are many more potential errors that could be detected and reported. For each and every type that is detectable by a JESD204B component, there should be a protocol test. These types of protocol tests can be a bit of a challenge to test and validate because a properly working link will never exercise them. They generally will require specialized test equipment. A BERT pattern generator can be used for many tests by creating a pattern that includes an error. Errors cases can also be generated using an FPGA with code modified to specifically generate those errors.

EMPHASIS AND EQUALIZATION TESTING

The JESD204B specification talks very little about emphasis and equalization. There are a few comments like "pre-emphasis might be required" and "equalization might need to be implemented," from which one can determine that the specification allows them but does not give any additional guidance. When using a converter with JESD204B that includes emphasis or equalization, how does one go about determining whether or not to turn it on and if so how much to turn it on? To answer that question, it is first best to understand the type of jitter called intersymbol interference (ISI). ISI is the name for the variation in edge timing that is caused by the filtering effects of a transmission line. Mathematically, it can be simply modeled as a low-pass filter. When sending high speed serial data down a transmission line, the filtering results in a distorted signal. Emphasis and equalization counteract the filtering effects of ISI with the goal of bringing the frequency response at the end of the channel back to as close to flat over frequency as possible and thus, resulting in a signal that is not distorted by ISI.

With a basic understanding of emphasis and equalization and ISI, the next step is setting them. What many people ask first is how long of a trace can be driven with and without emphasis/equalization. Real-world PCB designs have too many variables that can affect ISI to be able to specify the channel in terms of trace length. Variables like trace width, trace length, vias vs. no vias, dielectric material, connectors vs. no connectors, trace material, corners, passive components, and distance to ground plane can all affect channel performance. So, how can channel characteristics ever be correlated to emphasis/equalization? The solution is to specify the channel in terms of insertion loss. Insertion loss is described in the JESD204B specification as a measure of the power loss of a signal over frequency. Emphasis, equalization, and PCB channel can all be related in terms of insertion loss (and gain). Using a relevant frequency (the JESD204B specification lists ¾ baud rate) and an insertion loss limit (JESD204B lists −6 dB), the gain provided by emphasis and/or equalization can be selected to bring the frequency response at the selected frequency up above the loss limit. For example, a PCB channel with −12 dB of loss at +9 GHz would need +6 dB of emphasis/equalization gain to bring the total back up to −6 dB.

Alternately, converters manufacturers can provide a table of emphasis/equalization settings vs. PCB insertion loss. This method can result in a better solution, as it does not depend on as many assumptions. To build such a table for a transmitter (and to emulate end system designs), a set of test evaluation boards can be built with varying trace lengths.

The eye diagram at the end of the PCB trace can be directly measured and compared against the JESD204B Rx mask. By trying various PCB trace lengths, there will be one that results in the eye just barely passing the Rx mask. Since the insertion loss of that specific trace can be measured, the drive capability for a specific emphasis setting is known. Compare Figure 3 showing an eye diagram at the end of an ISI PCB to Figure 4, the eye diagram going into an ISI PCB. In this case, the data rate is 5 Gb/s, the ISI PCB has 8 dB of insertion loss at 4 GHz, and emphasis is off.

Repeating this process vs. emphasis settings will result in a table of emphasis settings vs. insertion loss. A similar approach can be done on a receiver with equalization. Start with a BERT generator that is outputting the maximum allowed total jitter (except for ISI jitter). Using the same set of ISI test boards with varying trace lengths, test with longer and longer traces until the receiver starts to get errors that exceed the target bit error rate (1E-15). Measure the insertion loss of the PCB trace. Repeat for every equalizer setting. In summary, if a JESD204B device manufacturer provides only emphasis/equalization gain, the first method can be used to pick settings. The best method is if the manufacturer provides a table of settings vs. channel insertion loss.

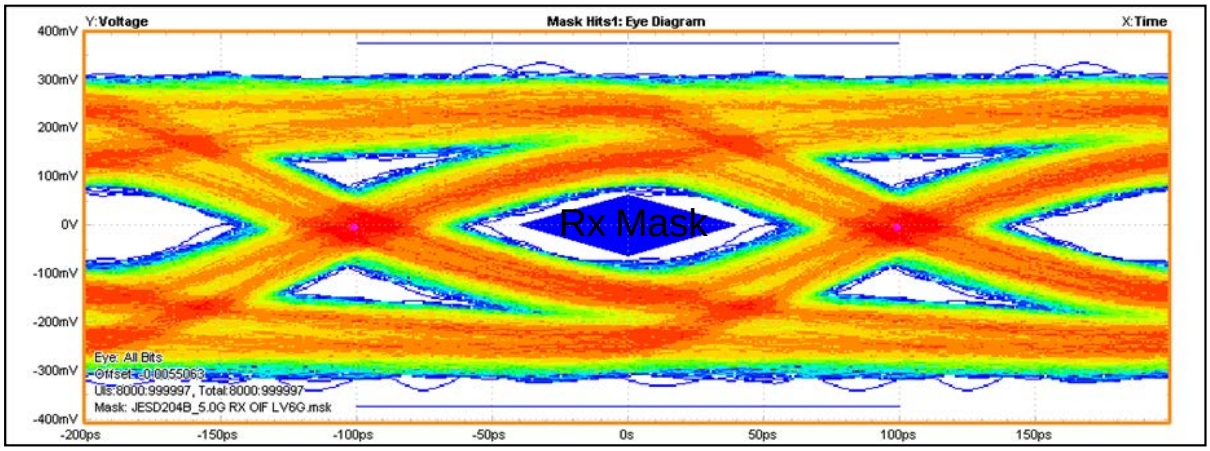


Figure 3. Eye Diagram at the End of a Long ISI PCB

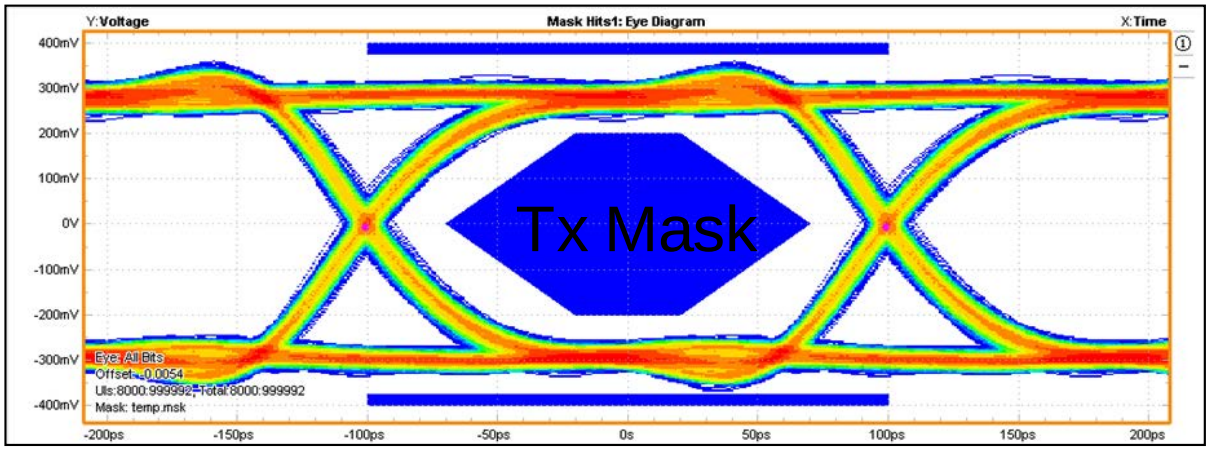


Figure 4. Eye Diagram Going into a Long ISI PCB

Should emphasis or equalization be used? From a frequency response correction standpoint, there's no clear reason to use one or the other. However, in most cases, emphasis can generate a certain amount of gain with less power. If system power is important, that could be a reason to choose emphasis over equalization. Another advantage of choosing emphasis over equalization is that the effect on the signal can be directly measured with an oscilloscope.

It can be common to have both a JESD204B Tx with emphasis and an Rx with equalization. How would you determine when to turn on both? Simply, if the insertion loss of the channel cannot be overcome by just emphasis or just equalization, then it's time to turn on both. As for how much gain to set each of them to, one advantage of specifying response in terms of insertion loss (and gain) is that it's additive. (For example, at the frequency of interest: a PCB trace with −20 dB of loss, a Tx with +6 dB of emphasis, and an Rx with +8 dB of equalization can be represented as −20 dB +6 dB +8 dB = −6 dB total).

EMULATING SYSTEM ENVIRONMENTS—NOISE AND JITTER

No end system design is free of noise and jitter. Emulating system jitter is fully specified in the JESD204B specification, but voltage noise is not. To emulate voltage noise in end system designs, component manufacturers can perform noise tolerance tests. One such test is power supply noise tolerance. For this test, noise is injected onto the components' various power supply domains. The amplitude of the noise is increased until the first compliance tests fails (often the first test to fail on a SerDes will be jitter). This test is repeated over the frequency range at which PCB noise is typically present (a few Hz to around 100 MHz). A plot of maximum power supply noise tolerated vs. frequency is generated. The same test can be performed on all other pins. The end result of all this testing is typically a set of practical PCB design recommendations, such as "keep a particular supply domain separated" or "use a bypass capacitor on this pin" or "don't route any signals near this pin".

MAINTAIN SIGNAL INTEGRITY WHEN MEASURING

As with any high speed serial test application, a number of best practices apply to ensure accurate measurement results, and you must be sure that your instrumentation offers sufficient performance and signal integrity to deliver accurate measurement results. Below are a few considerations:

Dynamic range: in general, it is best to use the full range of your oscilloscope's analog-to-digital dynamic range without clipping the amplifier. Although clipping might be acceptable when looking at a clock signal, doing this will hide ISI issues when evaluating data signals and can also affect the instrument's edge interpolation algorithm.

Sample rate: setting the oscilloscope to the highest sample rate provides the best timing resolution for the most accurate signal and jitter measurement. One exception would be if you are looking over longer time windows at lower timing accuracy.

Capture window: analyzing signals over a longer time window allows you to see low frequency modulation effects like power supply coupling and spread-spectrum clocking. Increasing the capture window unfortunately increases the analysis processing time. On SerDes systems, there is often no need to look at modulation effects below the loop bandwidth of the CDR that are tracked and rejected.

Test point access and de-embedding: ensure that you employ a mechanism for keeping the probe as close to the Tx test point as possible and as close to the Rx test point as possible. With high speed signaling test, timing, and amplitude measurements can seriously impact margin test results if the measurement process introduces unwanted signal discontinuity from long traces and/or fixturing from the actual Tx/Rx test points.

In some cases, the probe access point could be at a location where the signal is degraded due to the transmission line length. In this case, you might have to de-embed the transmission line to see what the real signal is. De-embedding involves recreating a model (using a linear method with S parameters) of the measurement channel between the instrument and the targeted test point. This model can be applied to acquired waveform data in the oscilloscope to account for those transmission line degradations (see Figure 5).

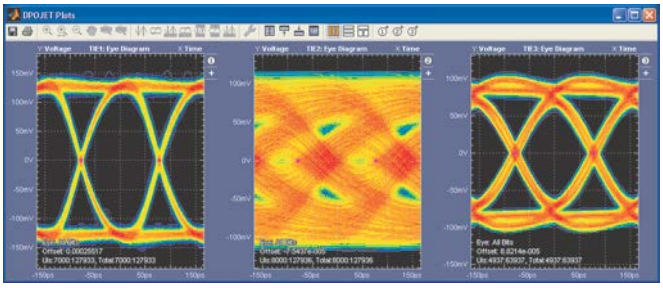


Figure 5. Eye Diagrams Illustrating Measurements Taken at Test Fixture, End of Channel, and Post-EQ

By practicing good signal integrity in your measurement techniques, you'll be better equipped to evaluate and characterize high speed technologies like JESD2024B.

SUMMARY

The recently released JESD204B interface can reliably increase data transfer bandwidth between a converter and a logic device, and a number of new devices using this interface are making their way to market. Unlike many other high speed serial interface standards, the JESD204B standard does not include an official compliance test specification, creating a number of challenges for system designers who must thoroughly test and debug their designs. Fortunately, the specification includes sufficient information to develop testing procedures, including PHY, timing, and protocol tests.

In addition to validating performance and compliance to the specification, testing can help determine the need for emphasis or equalization in a system design and help to identify unwanted sources of noise and jitter. As with any high speed serial testing effort, best practices for instrument selection, setup, and probing should be followed to ensure consistent and accurate results.

ABOUT THE AUTHORS

Frank Farrelly is a product engineering manager at Analog Devices. He has been with ADI for 19 years and is currently working on the characterization and validation of high speed SerDes products. He holds a BSEE degree from The University of Tennessee, Knoxville and an MBA from The University of North Carolina, Greensboro.

Chris Loberg is a senior technical marketing manager at Tektronix®, responsible for oscilloscopes in the Americas Region. Chris has held various positions with Tektronix during his more than 13 years with the company, including marketing manager for Tektronix' Optical Business Unit. His extensive background in technology marketing includes positions with Grass Valley Group and IBM. He earned an MBA in Marketing from San Jose State University.

REFERENCES

JESD204B specification.

OIF-CEI-02.0.

RESOURCES

Share this article on

One Technology Way • P.O. Box 9106 • Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 • Fax: 781.461.3113 • www.analog.com
Trademarks and registered trademarks are the property of their respective owners. TA11432-0-3/13

Slay Your System Dragons with JESD204B

by Ian Beavers, Applications Engineer, Analog Devices, Inc.

The JESD204B serial data link interface was developed to support the growing bandwidth needs of higher speed converters. A third generation standard, it provides a higher maximum lane rate (up to 12.5 Gbps per channel) while supporting deterministic latency and harmonic frame clocking. Additionally, it now can easily move large quantities of data for processing by taking advantage of higher performance converters that are compatible and scalable with open market FPGA solutions.

FPGA providers have been talking about multigigabit serialization/deserialization (SERDES) interfaces for many years now. In the past, though, most analog-to-digital converters (ADCs) and digital-to-analog converters (DACs) were not configured with these high speed serial interfaces. The FPGAs and the converters did not interface with any common standard that took advantage of the high SERDES bandwidth. JESD204B compliant converters can solve this problem, but this new capability introduces some questions.

What is 8b/10b encoding, and why is it needed on the JESD204B interface?

There can be no assurance of a dc balanced signal on a differential channel with random unencoded serial data, as there easily could be a larger number of either ones or zeros transmitted as opposed to the other. Random data that is sent across a serial link also has the potential to have long periods of inactivity or data that could be all ones or all zeros for a relatively long time.

When this happens, the dc balancing of an unencoded serial data stream becomes railed to one extreme or the other. At that point, when active data begins again, there is a strong potential for bit errors as the biasing of the lines is restarted. An additional long-term concern is electromigration, as a differential dc voltage is maintained on one side of the pair relative to the other. To counteract these issues, an 8b/10b encoding scheme is commonly used in differential serial data streams, including JESD204B.

In 8b/10b encoding, 10 bits are used to send the original 8 bits of information out of the source transmitter via a lookup table. This inherently accounts for a 25% inefficiency overhead (10b/8b = 1.25). In addition, the encoding allows for at least three but no more than eight bit transitions per 10-bit symbol. This ensures that there are enough transitions for the receiver to recover an embedded clock, regardless of the dynamic activity of the underlying data.

The disparity between the number of binary zeros and ones in the serial stream is kept to within ±1 using 8b/10b encoding, so the signal maintains a dc balance over time. The converse decoding of 10 bits to 8 bits must then be performed on the data stream at the receiver side to be able to recover the original data using the reverse lookup table. A more efficient 64b/66b encoding that operates on a similar principle, but with only a 3.125% overhead, is more advanced and has the potential to be used in future generations of JESD204.

The assigned JESD204B lanes of my converter do not route easily to my FPGA on my system board. There are crisscrossing pairs all over the place and it is generally susceptible to crosstalk. Is there a way to remap the assignment of the JESD204B lanes to make my layout easier?

Although converters may have JESD204B serial lanes defined by a number, letter, or other nomenclature to designate their particular relevance in the complete link, they are not required to be fixed. The specification allows for remapping of these assignments in the initial configuration data, as long as each lane and device has a unique identification. The link configuration data includes the device and lane identification numbers to identify its operation. With this information, a multiple lane transmitter could easily reassign any digital logical serial data to any physical output lane using a crossbar mux.

While it is an optional feature that the specifications allow, if an ADC vendor has a crossbar mux feature to reassign logical to physical output assignments, then the link I/O can be reconfigured in the best order for the easiest layout. The FPGA receiver can take the same initial configuration data and change the expected lane assignments to recover the data. With this ability, the routing of lanes from one device to the other can be made much easier and independent of the initial named assignment by the silicon vendor in the data sheet.

I am looking at potentially designing a converter into my system that uses a JESD204B multipoint link. How is it different from a single link?

The JESD204B specification makes provisions for what is known as a multipoint link interface. This is a communications link that connects three or more JESD204B devices. This link configuration can make sense over a single

link in some cases, depending upon how the converter is being used.

Take, for example, a dual ADC that uses JESD204B. In most cases, a dual ADC would have a single clock input to both converters. This would force simultaneous analog sampling at the same frequency. But for some unique applications, such a device could also use two separate input clocks, where each clock could drive its respective ADC independently. This would allow for a sampling phase difference between the two ADCs, or even for each ADC to be sampled with a noncoherent frequency with respect to the other. In the latter case, a single JESD204B link with data from both converters would not operate correctly without a complex back-end FIFO scheme.

A solution to this problem could be to have the dual converter use a multipoint link JESD204B interface, where each converter channel uses its own serial link output. Noncoherent clocks then could be used on each ADC, and each serial link output could easily route independently to a separate FGPA or ASIC. A multipoint link configuration can also be used when sending multiple streams of data from a single FPGA to several DACs. Device clock distribution skew can be more challenging to minimize within a multipoint configuration as the number of devices within the link grows.

What exactly is deterministic latency within JESD204B? Is this the same as the total latency of my converter?

The total latency of an ADC is the time it takes an analog sample to be clocked in, processed, and output digitally from the device. Similarly, the total latency of a DAC is the time from when the digital sample data is clocked into the part until that corresponding sample is clocked out of the analog output. Typically, these are both measured in sample clock periods of resolution, as they are frequency dependent. This is fundamentally not the same definition as the deterministic latency described by a JESD204B link implementation.

Deterministic latency across the JESD204B link is defined by the time it takes data to propagate from the parallel framed data input at the transmitter (ADC or source FPGA) to the parallel deframed data output at the receiver (DAC or receiver FPGA). This time is typically measured in either frame clock periods of resolution or device clocks (Figure 1). The definition excludes the analog front-end core of an ADC and the back-end analog core of a DAC. Not only are two devices a function in this latency computation, but so is the serial data signal routing interfacing the two. This means that the deterministic latency could be larger or smaller within a multiconverter system or multipoint link, depending upon the length of the JESD204B lane routing. Buffer delays on the receiver can help account for latency differences due to routing.

How are tail bits used in JESD204B, and what is their purpose?

The JESD204B link allows for more information space to be allotted than may actually be needed to send the converter data and control bits. If data for a particular converter or configuration does not fill up the entire space, then this "padding" is filled with what are defined as tail bits. Take, for example, a case where a space of N' = 16 is more than the parceled 13 bits of real data (N = 13 + CS = 0). Three tail bits would be used to fill the unused data space (Figure 2).

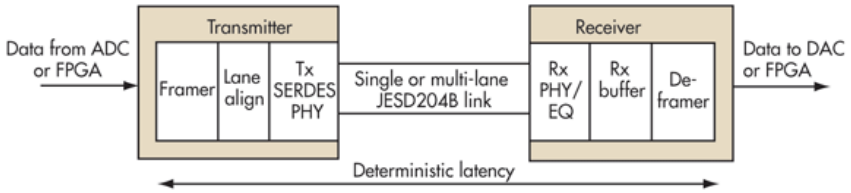


Figure 1. A Conceptual Example of JESD204B Deterministic Latency Between Framer and Deframer on Two Linked Devices. The Latency Is a Function of Three Items: the Transmitter, the Receiver, and the Interface Propagation Time Between the Two

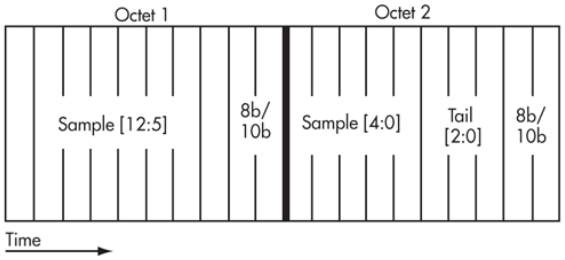


Figure 2. Three Tail Bits Can Be Used to Pad and Fill a Second Octet for N' = 16 When a Converter Only Uses 13 Bits of Sample Data

Tail bits are informationless dummy bits and are only used to completely pad the unused space. Since tail bits have the potential to cause unwanted spurious noise if they are all assigned a recurring static value, they also can be optionally represented as a pseudorandom sequence. Both the transmitter and receiver must understand that these bits are informationless based on the link configuration. The receiver can therefore simply discard them from the stream of relevant data.

My link patterns work fine, but I am not getting converter data transmitted in a normal operating mode. In past generations of converters, low voltage differential signaling (LVDS) and parallel interfaces allowed easy probing/debugging of a least significant bit (LSB) or most significant bit (MSB) pin of a DAC or ADC to see if the functional converter operation was taking place. How can I probe an MSB or LSB when using the JESD204B interface?

This is one of the few drawbacks to the JESD204B interface. It is not easy to electrically probe an LSB or MSB I/O to see if there is correct activity to and from the converter. This is because the sample data is serialized per channel, so a particular weighted bit cannot easily be probed electrically. However, a few options can be used to debug a system issue when you quickly want to know what, if any, valid data is being sent or received from your converter.

Some oscilloscope vendors provide real-time data processing to serially decode 8b/10b data and display an unencoded stream on the oscilloscope screen. Unscrambled data can be probed in this fashion to determine what activity is taking place on the link.

FPGA vendors offer an internal probing software tool that gives system designers a method to observe the I/O data sent and received from within the FPGA by connecting it via a USB dongle to a computer. Also, some ASICs and converters offer an internal serial loop-back self-test mode that can be used to help decipher data issues on the link.

How do I calculate the lane rate for my converter, given that I know the other parameters of the link?

System designers using JESD204B can easily compute the number of lanes or lane rate for their link given that they know the other key criteria of their converter, ASIC, or FPGA. There is a mathematical relationship for all of the basic link parameters below such that one unknown variable can be computed and solved. Based on the result, system designers can choose other parameters to change the link operation within the confines of the converter or FPGA architecture:

$$\textit{Lane rate} = (M \times N' \times [10/8] \times Fs)/L$$

where:

M is the number of converters on the link.

N' is the number of informational bits sent in a sample (including sample resolution, control and tail bits).

Fs is the device or sample clock.

L is the lane count.

Lane rate is the bit rate for a single lane.

10/8 is the link overhead due to 8b/10b encoding.

For example, consider a dual ADC with N' = 16, Fs = 235 MHz, using two lanes. What is the lane rate?

$$\textit{Lane rate} = [2 \times 16 \times 1.25 \times 235 \text{ MHz}]/2$$

$$\textit{Lane rate} = 4700 \text{ Mbps or } 4.7 \text{ Gbps}$$

What is an application layer, and what does it do?

An application layer is a method provided for in JESD204B that allows sample data to be mapped outside the normal specification. This can be useful for certain converter modes that need to pass data samples in sizes that are relatively different from the N' of the link.

An otherwise inefficient arrangement on the link can be made more efficient with a lower lane count or lower lane speed by using an application layer. Both the transmitter and receiver need to be configured to understand a specific application layer, as it can be custom or uniquely designed by a particular converter mode. Figure 3 shows an example where five samples are partitioned into a space typically occupied by only four.

When using the equation from the previous question for application layer calculations, the effective N', instead of the actual N', needs to be used. For example, in the application layer case shown below, although the actual JESD024B sample N' is 16, the effective N' for ADC samples can be figured since 64 bits are used to send five samples. Therefore, Neff = 64/5 = 12.8. With all other variables held equal, the lane rate could then be run 20% slower:

$$Neff/N' = 12.8/16 = 0.8.$$

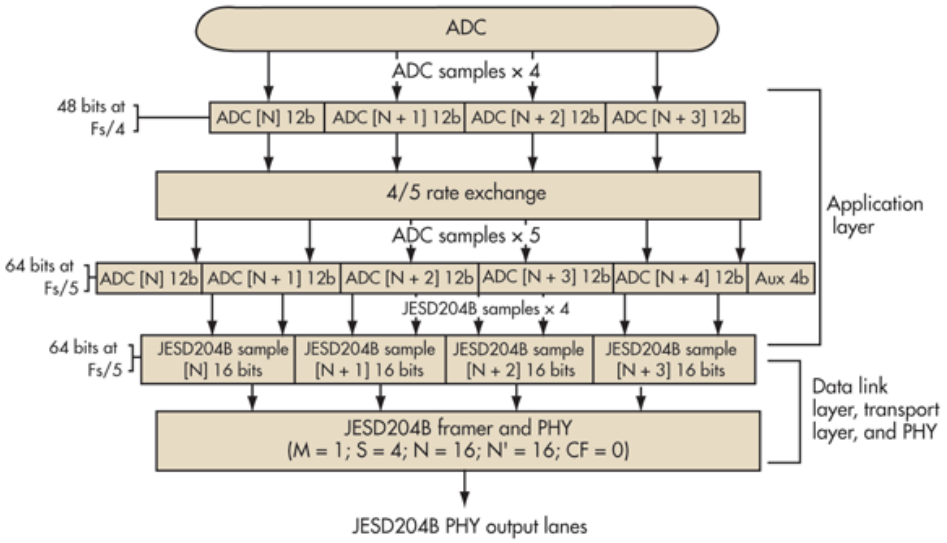


Figure 3. An ADC Application Layer Can ReMap Five 12-Bit ADC Samples into the Space Used by Four JESD204B N' = 16 Samples. Four Bits of Extra Auxiliary Information Can Be Made Available for Additional Use

What's next?

As JESD204B continues to proliferate within the data converter market, intellectual property (IP) capabilities on FPGA platforms should help speed its adoption. Future discussions on the subject should only grow, albeit with additional complexity, as more engineers become involved and start designing new systems.

ABOUT THE AUTHOR

Ian Beavers is an applications engineer for the High Speed Converters team at Analog Devices, Inc., Greensboro, N.C. He has worked for the company since 1999. He has more than 15 years of experience in the semiconductor industry. He earned a bachelor's degree in electrical engineering from North Carolina State University and an MBA from the University of North Carolina at Greensboro. He can be reached at Ian.Beavers@analog.com.

REFERENCES

JESD204B. www.analog.com/jesd204.

RESOURCES

Share this article on

One Technology Way • P.O. Box 9106 • Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 • Fax: 781.461.3113 • www.analog.com
Trademarks and registered trademarks are the property of their respective owners. TA11717-0-7/13

JESD204B Subclasses (Part 1): An Introduction to JESD204B Subclasses and Deterministic Latency

by Del Jones, staff applications engineer—high speed converters, Analog Devices, Inc.

1 INTRODUCTION

Unquestionably, a hallmark of the Information Age is an explosion in the need to collect, process, and distribute larger and larger chunks of data. In communications networks, this means more bandwidth for the infrastructure and the components connecting to it. In the medical industry, this translates into more detailed information from scans, X-rays, and other instruments. Relatedly, testing and analysis of this rapid expansion in bandwidth translates into the need for higher speed and capacity in electronic test equipment.

This insatiable demand for data is what led to the need for JEDEC to introduce the JESD204 standard for a high speed serial link between data converters and logic devices. The "B" revision of the standard, released in 2011, has pushed the serial link data rates to 12.5 Gbps in order to enable the higher bandwidth requirements of today's converter-based applications. In many of these applications, there is a need for data to traverse through the system with a known and consistent delay from power cycle to power cycle. This concept is referred to as "deterministic latency" and provisions for this requirement were introduced in the JESD204B standard as well. Prior to the release of this revision, designers of systems needing deterministic latency used external application layer circuitry to realize the requirement. In the JESD204B standard, three subclasses are introduced. Subclass 0 is intended to be backward compatible with the JESD204A standard and has no provision for implementing deterministic latency. Subclass 1 introduces an external reference signal, called SYSREF, which provides a system-level reference for sample timing. Subclass 2 defines how the SYNC~ signal can be used as the system-level reference for sample timing. In each case, it is the sample timing reference that can be used to implement deterministic latency. The intent of this "mini tutorial" is to clarify the operational distinctions between the three JESD204B subclasses, and to provide the reader with a working knowledge on the implementation of their individual deterministic latency functionality.

Designers of systems needing deterministic latency used external application layer circuitry to implement this requirement prior to the release of this revision.

2 A DETERMINISTIC LATENCY OVERVIEW

The JESD204B standard defines deterministic latency (DL) as the time difference between when frame-based samples arrive at the serial transmitter to when the frame-based samples are output from the serial receiver. Latency is measured in the frame clock domain and must be programmable in increments at least as small as the frame clock period. The latency must be repeatable from power-up cycle to power-up cycle as well as with any resynchronization event. This definition is illustrated in Figure 1.

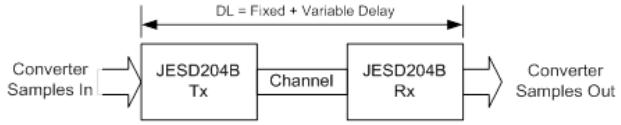


Figure 1. Deterministic Latency Illustration

The deterministic latency in a JESD204 system consists of fixed delays and variable delays. Variable delays are the result of arbitrary phase relationships from power cycle to power cycle between clock domains in the digital processing blocks. In JESD204A and JESD204B subclass 0 systems, the variable delays cannot be accounted for. Therefore, there is a power cycle variation in the latency across the link.

3 SUBCLASS 0

Subclass 0 is primarily provided in the JESD204B standard to ensure backward compatibility to JESD204A devices. This could be desirable if system designers have a custom ASIC with a legacy JESD204A interface that they want to connect to a JESD204B converter with updated features.

3.1 REQUIREMENTS FROM THE JESD204B STANDARD

The JESD204B standard provides requirements and recommendations for operating in subclass 0 mode that may differ from the requirements for the other subclasses. Most notably, the requirements for the SYNC~ signal are unique from subclass 1.

SYNC~ requirements (also applies to subclass 2):

- The SYNC~ output from the JESD204B receiver must be synchronous with the receiver's frame clock

- It is also required that the transmitter's frame clock be synchronous to SYNC~; this can be achieved by allowing the SYNC~ input of the transmitter to reset the frame clock counter; the delay from the SYNC~ input to the frame clock boundary must be specified

- Recommended to use same logic as for device clock (LVDS, for example)
- Must not be ac-coupled
- The device clock to SYNC~ delay (tDS_R) at the receiver device pins must be specified
  - In a system where the frame clock is faster than the device clock, SYNC~ is launched and captured using the frame clock; regardless, tDS_R is still specified
- The setup and hold times for SYNC~ to the device clock at the transmitter must be specified

3.2 IMPLICATIONS OF SUBCLASS 0 OPERATION

Lane alignment within a single JESD204 link is handled automatically in the JESD204 receiver through the use of an elastic buffer on each JESD204 lane. During the initial lane alignment sequence (ILAS), all lanes are monitored and when the last arriving lane's "start of multiframe" alignment control character arrives, all buffers are released simultaneously. This is illustrated in Figure 2.

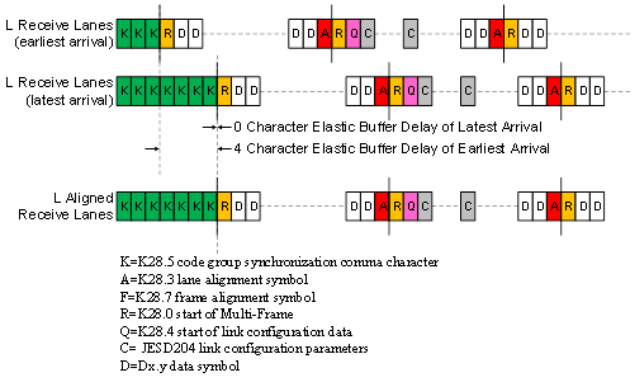


Figure 2. Lane Alignment within a Single Link

Although it is recommended that the frame clocks from the receiver and transmitter both be synchronous to the SYNC~ signal (see SYNC~ requirements above), there is no mechanism to synchronize the local multiframe clocks (LMFC) across the system. Therefore, link alignment across multiple converter devices is not possible using deterministic latency methods. Conversely, multiple converters within a single device configured as part of a single JESD204B link can be aligned without external circuitry. The LMFC misalignment will contribute up to one LMFC of variable latency to the total latency of the link.

3.3 A SUBCLASS 0 SOLUTION FOR MULTICHIP SYNCHRONIZATION

One advantage of implementing deterministic latency is that it provides a means by which multichip synchronization can take place. However, it is not necessary to implement deterministic latency to achieve multichip synchronization. The JESD204 standard makes provisions for "control bits" to be added to sample data in order to convey information about the sample from the transmitter to the receiver. In ADC applications, it is possible to use a control bit as a "time stamp" to flag a sample that occurs coincidently with an external reference. If using a subclass 1 device in subclass 0 operating mode[1], this can be accomplished using the SYSREF input. It is also possible to use the SYNC~ signal in multiADC applications connected to a single logic device. The basic requirement for multichip synchronization is to have an external reference for the ADCs and support for control bits in the JESD204 transmitter.

ADI's AD9625 and AD9680 are devices that support the time stamp feature for multichip alignment. Figure 3 shows an example of how the SYSREF input can be used to time-stamp the sample that is coincident with this external reference. As illustrated, when the SYSREF is sampled by the device clock, the designated control bit is set in that sample. This can be done for every device in the JESD204B system.

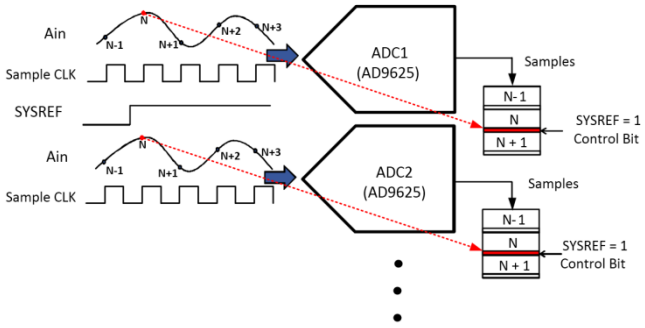


Figure 3. Adding a Time Stamp Control Bit on Multiple ADCs

Once the samples from each of the ADC devices are time stamped, the downstream logic device can align the samples as illustrated in Figure 4.

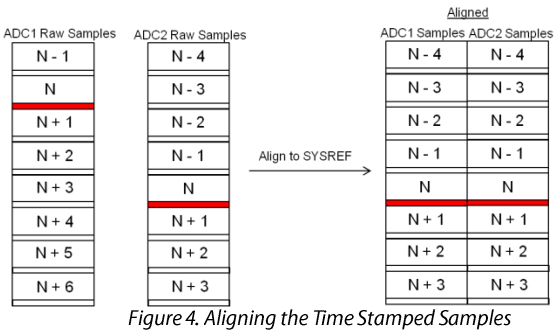


Figure 4. Aligning the Time Stamped Samples

[1] Not using the SYSREF input for deterministic latency.

4 SUBCLASS 1

Lane alignment within a link and multichip alignment is realizable while operating in subclass 0 mode as previously mentioned. However, there are many applications that depend not only on synchronizing samples from multiple devices, but also require a known, deterministic delay for data traversing between the converter and the logic device. For example, some ADC applications use a feedback loop to calibrate the front-end analog gain. Often this is done using a test input signal into the receiver. The digitized data is then used to determine any adjustments that are needed. It is critical to know the latency from the analog input to the logic device that is making the adjustment decision. The arrival time of this data needs to be the same after every power cycle and regardless of synchronization events. In these applications, deterministic latency must be implemented.

In a subclass 0 system, the sample data is released from the JESD204B receiver after the arrival of the latest lane. However, the release time can vary from one power cycle to the next. In a subclass 1 system, a "receive buffer" is defined whose release time is referenced to the external SYSREF signal. Therefore, it is not subject to the power cycle variations that are encountered in the JESD204B system. This concept is illustrated in Figure 5.

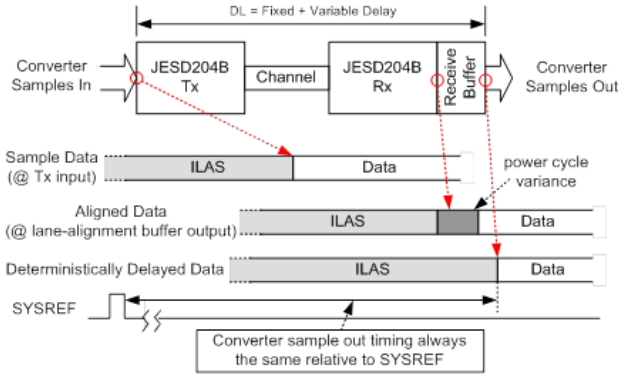


Figure 5. Data Release Timing Using SYSREF in a Subclass 1 System

The buffer release time is referenced to the SYSREF signal through its relationship to LMFC. SYSREF is used to phase-align the LMFCs across all of the JESD204B devices in the system. The buffer release time is referenced to this SYSREF-aligned LMFC.

4.1 SYSTEM REQUIREMENTS AND GUIDELINES FOR IMPLEMENTING SUBCLASS 1

The accuracy and reliability of deterministic latency in the JESD204B system relies on the relationship between the device clock and SYSREF. The device clock is the system reference clock from which the sample clock (typically), JESD204B clock, and serializer clock are derived. It is used to capture SYSREF and phase align the leading edge of the frame and multiframe clocks as illustrated in Figure 6. The JESD204B standard provides requirements and recommendations for SYSREF and device clock. The standard also provides guidelines regarding PCB layout and system timing. However, how these requirements get implemented in a JESD204B system depends on the application's system level requirements, such as deterministic latency uncertainty (DLU). Determining DLU and other details of the application specific implementation will be covered in detail in "JESD204B Subclasses (Part 2): Subclass 1 vs. Subclass 2 System Considerations."

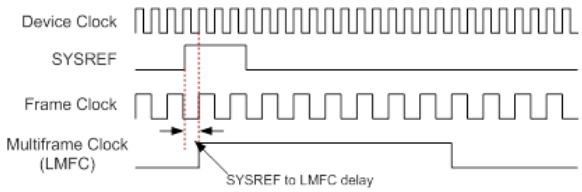


Figure 6. Phase Alignment of Frame Clocks Using SYSREF

Other key requirements and suggestions for subclass 1 operation:

- The delay from the leading edge of SYSREF to the frame and multiframe boundary must be specified for all devices in the JESD204B system. In ADI converter products, this is referred to as the SYSREF-to-LMFC delay.
- The receive buffer is used to buffer data and uses the SYSREF aligned LMFC as a deterministic reference for releasing data. The JESD204B standard defines what is called the receive buffer delay (RBD). The RBD is what determines the buffer depth and is specified to be between 1 and k frame cycles (TF). The RBD is used to compensate for variable delay in the system. As the number of frames in a multiframe increases, more variable delay can be tolerated. ADI DAC devices support k values of 16 or 32. A setting of 32 is recommended for most applications.
- Since it is likely that the exact implementation for deterministic latency will vary from one manufacturer to the next and even different devices from the same manufacturer, it is important to use the same model of converter when multichip synchronization is required in your system.
- It is also important that inter device lane skews be minimized. For ADI DAC applications, the

combination of inter device skew plus the maximum variable delay should be less than the period of the local multiframe clock (LMFC).

- Device clock and SYSREF should be generated from the same device to ensure the phase alignment of the two signals. The inter device skew for both SYSREF and device clock should also be minimized.
- The concept of SYNC~ combining is presented when discussing subclass 0 operation and multichip synchronization. For a subclass 1 system, this is not necessary.

4.2 SYSREF AND DEVICE CLOCK

The SYSREF signal can be a single pulse, a periodic square wave, or a gapped periodic square wave. The period of the SYREF must be an integer multiple of the LMFC. ADI devices support all three types of SYSREF signal.

The timing of the SYSREF signal must be accurately controlled with respect to the device clock such that the device clock sampling edge is fixed and known by the user. As already mentioned, the SYSREF signal must be source synchronous with the device clock. Therefore, it is recommended that SYSREF generation is created by the same device that delivers the device clock throughout the system. The AD9525 is one ADI device that is suitable for this task.

The clock distribution skew and other skew requirements in the JESD204B standard are more like guidelines instead of rules. They were introduced to make a case for the amount of deskew capability to recommend for the deserializer. You can find these described in section 4.12 of the JESD204B standard. A practical guide to determining SYSREF and clock skews is presented in "JESD204B Subclasses (Part 2): Subclass 1 vs. Subclass 2 System Considerations."

5 SUBCLASS 2

Rather than using an external signal to provide a timing reference, subclass 2 systems use the SYNC~ signal to provide deterministic latency and multichip synchronization. The main advantage to this implementation is that it reduces the pin and net count in the JESD204B system. Recall that the idea behind SYSREF in subclass 1 is that it is used to synchronize the internal frame and multiframe clocks (LMFCs) across all devices in the system. Since SYNC~ is generated based on the receiver's LMFC, it carries the LMFC timing information that can be used to achieve the same synchronization between receiver and transmitter as if an external reference were used. Additional functionality and precision are required for the SYNC~ than that of the subclass 1 SYNC~. These requirements and the system synchronous timing requirements result in lower achievable device clock frequency. This will be covered in more detail in "JESD204B Subclasses (part 2): Subclass 1 vs. Subclass 2 System Considerations."

The challenges to meet the timing requirements while using SYNC~ as the timing reference are similar to those when using SYSREF. The system timing accuracy is limited to the distribution skew of the SYNC~ and device clock on the PCB, as well as their propagation delays. The resolution of the accuracy will depend on the device clock period. As with subclass 1, the system DLU requirement will determine the distribution skew limitations.

In a subclass 1 system, the device clock/SYSREF source is the master reference with synchronization requests coming from the logic device. In a subclass 2 system, the logic device is the master timing controller and is responsible for corrections to the LMFC phase on either side of the link. How this is achieved depends on whether the system is a DAC-based or ADC-based system.

5.1 ADC SUBCLASS 2 IMPLEMENTATION OVERVIEW

In a subclass 2 ADC application, the SYNC~ deassertion is captured by the detection clock, which is typically the device clock, and is used to reset the phase of its LMFC. Upon detecting and capturing the SYNC~, besides resetting its local LMFC, the JESD204B transmitter will begin transmitting K28.5 characters and will continue to do so until the system clocks have settled. The ILAS portion of the synchronization process will commence on the LMFC boundary after the clocks have settled. In an ADC system, the alignment of the ADC's LMFC is not an iterative process and is accomplished with a single SYNC~ assertion as illustrated in Figure 7. A periodic SYNC~ can also be used to monitor phase alignment of the transmitter's LMFC. Refer to section 6.4 of the JESD204B standard for more details.

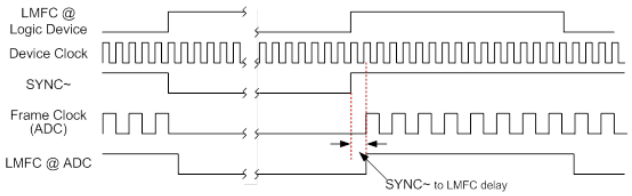


Figure 7. Phase Alignment of Frame Clocks Using SYNC~

5.2 DAC SUBCLASS 2 IMPLEMENTATION OVERVIEW

In subclass 2 operation, the logic device's LMFC is the master LMFC reference and the converter LMFC must be phase aligned to it. In a subclass 2 DAC application, the logic device also uses the detection clock (typically, the device clock) to capture the SYNC~ from one or more DAC devices. The logic device will detect the phase difference

[1] Not using the SYSREF input for deterministic latency.

between its own LMFC and the DAC LMFC and will issue adjustment commands to the DAC during the ILAS portion of synchronization. The ILAS is four multiframes long and the link parameters, including LMFC phase adjustment information, is transmitted to the receiver during the second LMFC period. The LMFC phase adjustment commands that are given by the logic device to the DAC(s) in the JESD204B system are given below:

- PHADJ (phase adjust): This command indicates whether a phase adjustment is needed or not.
- ADJCNT (adjustment count): This command indicates the number of adjustment steps that are needed.
- ADJDIR (adjustment direction): This command indicates if the LMFC phase should be advanced or delayed.

Depending on the adjustment clock resolution and its relation to the LMFC period, it is possible that the adjustment of the DAC's LMFC will take more than one ILAS period. After any phase adjustment is performed on the DAC, it issues an error report by asserting the SYNC~ low. The transmitter on the logic device will use this reassertion to detect the LMFC phase difference again. If no further adjustment is needed, then the PHADJ bit is reset during the ILAS and no error report is issued by the receiver. At this point, the LMFCs are aligned and user data transmission can commence. If another adjustment is needed, the logic device transmitter will initiate another iteration of the process. Refer to section 6.4 of the JESD204B standard for more details.

Once the LMFCs across all of the devices in the JESD204B system are phase aligned, deterministic latency is achieved through the same methods as subclass 1. That is, the release time of the receive buffer is referenced to the phase aligned LMFC instead of the nondeterministic arrival time of the last arriving lane data as illustrated in Figure 5. The only difference is in how LMFC phase alignment is achieved.

5.3 SYSTEM REQUIREMENTS AND GUIDELINES FOR IMPLEMENTING SUBCLASS 2

The accuracy and reliability of deterministic latency in the JESD204B system relies on the relationship between the device clock and each of the SYNC~ signals in the JESD204B system. As with subclass 1, the device clock is the system reference clock from which the sample clock, JESD204B clock, and serializer clock are derived. It is used to capture SYNC~ which provides information to the logic device regarding the LMFC phase relationships across the system. The JESD204B standard provides requirements and recommendations for subclass 2 operation as summarized below.

- For ADCs:
  - ADC must adjust its internal frame clock and LMFC (and possibly sample clock) relative to detected SYNC~ from logic device
  - Resolution of the LMFC adjustment should be defined by device manufacture and will limit system synchronization accuracy
  - SYNC~ detection resolution should be defined by device manufacture and will limit system synchronization accuracy.
  - Delay from SYNC~ deassertion to ADC LMFC boundary as illustrated in Figure 7 must be specified
- For DACs:
  - DAC must be able to adjust its internal Frame clock and LMFC as directed by the logic device (as described in the DAC Subclass 2 Implementation Overview section above)
  - DAC LMFC adjustment resolution must be specified (in DAC device clock periods)
  - The DAC must issue an error report whenever a phase adjustment has been made
- For logic devices in a DAC application:
  - Must be able to detect the phase of SYNC relative to its own LMFC in increments of the detection clock (typically the device clock)
  - Must be able to calculate ADJCNT based on the DAC adjustment resolution
  - Must be able to send corrective information to DAC during ILAS (as described in Table 1)

6 FINAL THOUGHTS

To meet the demands for faster data processing capability in the applications of today and tomorrow, JESD204B defines the multigigabit interface as a required communications channel between data converters and logic devices. Determining which subclass your application needs is an important step in your system design. For those systems not requiring deterministic latency, any of the three subclasses will suffice but subclass 0 will be the least problematic to implement. If deterministic latency is a requirement, other system level considerations should be considered for subclass 1 or subclass 2 designs. In "JESD204B Subclasses

(Part 2): Subclass 1 vs. Subclass 2 System Considerations," we will take closer look at some of these issues to help system designers make an informed decision regarding which subclass of JESD204B is appropriate for their design.

RESOURCES

Share this article on 

One Technology Way • P.O. Box 9106 • Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 • Fax: 781.461.3113 • www.analog.com
Trademarks and registered trademarks are the property of their respective owners. TA12594-0-7/14

JESD204B Subclasses (Part 2): Subclass 1 vs. Subclass 2 System Considerations

by Del Jones, staff applications engineer — high speed converters, Analog Devices, Inc.

1 INTRODUCTION

In "JESD204B Subclasses (Part 1): An Introduction to JESD204B Subclasses and Deterministic Latency," a summary of the JESD204B subclasses and deterministic latency was given along with details regarding an application layer solution for multichip synchronization in a subclass 0 system. Part 2 of the series takes a closer look at the differences between subclass 1 and subclass 2. In particular, we will look at the challenges to meeting the deterministic latency related timing requirements, device clock speed limitations in subclass 2, and guidelines on which subclass is best for a given system application.

2 SUBCLASS 1

In a subclass 1 system, the accuracy of the deterministic latency depends on the timing relation between device clock and SYSREF and the distribution skews of these signals within the system. In addition to the setup and hold time requirements for SYSREF (T_{SU} and T_{HOLD}), the application's tolerance for deterministic latency uncertainty will be critical in defining the application's distribution skew requirements for SYSREF and device clock.

2.1 CAPTURING SYSREF ACCURATELY

Converters employing the JESD204B interface sample data at a very high rate. In order to reduce phase noise in the system, it is common for these converters to use a reference clock, which is the same as the JESD204 device clock, that is at or above the sample rate. In many cases, this clock is in the GHz range. At these speeds, meeting the setup and hold time requirements become very challenging. To ease the system design, it may be necessary for the phase offset of SYSREF and/or device clock to be programmable for each device that is part of the JESD204B system.

One advantage that subclass 1 has over subclass 2 is that it uses source synchronous clocking. A subclass 2 system uses system synchronous clocking and will encounter frequency limitations sooner than that of one that uses source synchronous clocking. This will be demonstrated when we take a closer look at specific subclass 1 and subclass 2 timing examples.

2.2 DETERMINISTIC LATENCY UNCERTAINTY

Deterministic latency uncertainty (DLU) is the LMFC skew in the JESD204B system and is determined by the difference between the earliest and latest possible capture of SYSREF in the system. Figure 1 illustrates the worst case DLU that occurs when setup and hold time requirements for SYSREF capture are not met at every device in the system[1]. This occurs when the distribution skew of the device clocks in the system are not controlled and creates up to one device clock (DCLK) of uncertainty. This is added to the SYSREF distribution skew (DS_{SYSREF}) to produce the total DLU.

$$DLU = DS_{SYSREF} + T_{DCLK}$$

DS_{SYSREF} is the difference in the arrival time of the earliest arriving SYSREF in the system (across all devices in the system) and the last arriving SYSREF. In the illustration, T_{SU} is ½ T_{DCLK} and T_{HOLD} is ¼ T_{DCLK}. The earliest arriving SYSREF (A) is captured at the earliest possible time ($DCLK_A$ just meets the setup time requirement) while the last arriving SYSREF (N) is captured at the latest possible time ($DCLK_N$ just misses the setup time requirement). So the corresponding LMFCs are misaligned by $DS_{SYSREF} + T_{DCLK}$.

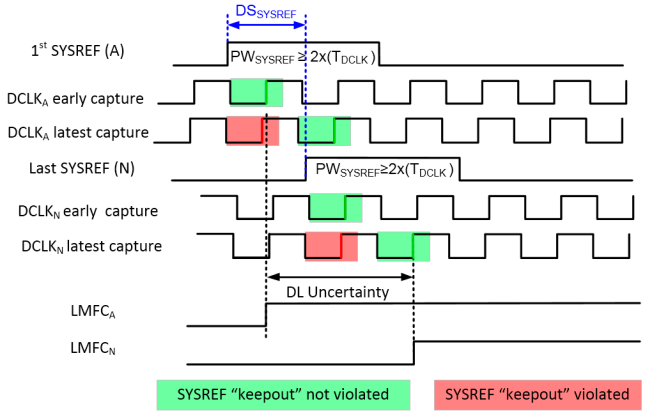


Figure 1. Worst Case Deterministic Latency Uncertainty

In many applications, the requirements for DLU are such that this worst case scenario is acceptable. For these applications, it may not be necessary to tightly control the device clock distribution skew. Ensuring the pulse width of SYSREF is ≥ (2 × T_{DCLK}) and controlling the SYSREF distribution skew to meet the system timing requirement should be adequate.

[1] In order to keep the illustration of the concept of DLU simple, clock jitter and variations due to process, voltage, and temperature (PVT) are not considered here.

In applications where the additional device clock of uncertainty is not acceptable, then the device clock distribution skew must be tightly controlled to ensure that the timing requirements for SYSREF are met at each device in the system. This case is illustrated in Figure 2 and the uncertainty is given by the equation:

$$DLU = DS_{SYSREF} + T_{\text{“Valid Window”}}$$

$$\text{where } T_{\text{“Valid Window”}} = T_{DCLK} - (T_{SU} + T_{HOLD})$$

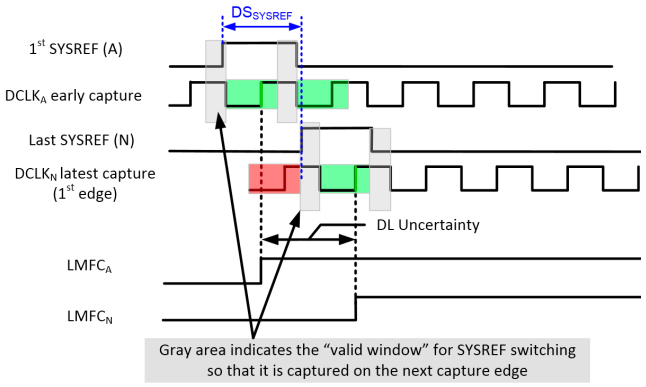


Figure 2. DLU While Meeting Setup and Hold Time for SYSREF

2.2.1 MINIMIZING DETERMINISTIC LATENCY UNCERTAINTY

As implied by the equation for DLU above, DLU can be minimized by ensuring that setup and hold time are met for each SYSREF/DCLK pair and by minimizing the interpair distribution skew.

To meet the setup and hold time requirements, each device in the JESD204B system should have its own SYSREF/DCLK pair. Within each of these pairs, trace length matching can be employed to ensure timing. The limit for matching trace lengths is determined by the valid window time for SYSREF switching. Also, SYSREF should be output with the capture edge of DCLK and the SYSREF length must be greater than the DCLK length as determined by the hold time requirement (if T_{HOLD} is 0, then the lengths can be equal).

Since trace length matching is employed, minimizing the interpair distribution skew is effectively the same as minimizing the SYSREF distribution skew. The limit for this distribution skew is the DLU limit minus the valid window time and can also be managed through trace length matching. The DLU limit is set by the requirements of the application.

These methods for minimizing DLU are illustrated in Figure 3. Since each device in the JESD204b system has its own SYSREF/DCLK pair, meeting the timing requirements for capturing SYSREF is just like any system that uses source synchronous clocking. Timing margins at each device are considered independently of the other devices in the system.

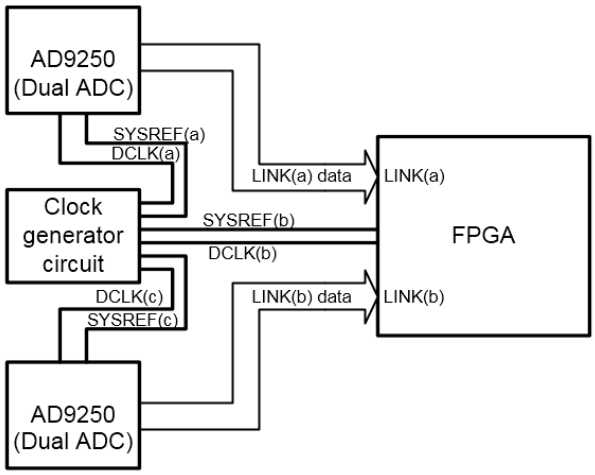


Figure 3. SYSREF/DCLK Routing for a 3-Device JESD204B System

2.2.2 SYSREF TIMING EXAMPLE USING THE AD9250

The AD9250 is a 14-bit, 250 MSPS dual ADC with JESD204B serial data output specified at 5 Gbps. To maximize PLL performance, the AD9250 can accept device clock speeds as high as 1.5 GHz. This provides an excellent example to use to demonstrate how to meet SYSREF timing using trace length matching under the most stringent system DLU requirement[2]. Here are the conditions for the example:

- DCLK = 1.5 GHz (667 ps period)
- T_{SU} = 500 ps and T_{HOLD} = 0 ps
- For the example, the system's DLU_{MAX} = 1 DCLK (667 ps)

INTRAPAIR TRACE LENGTH MATCHING TO MEET SYSREF TIMING

Based on specifications for the example, the “valid window” for meeting setup and hold time is 167 ps (667 ps T_{DCLK} – 500 ps T_{SU}). Travel time is the time from a signal leaving the source to arriving at the sink. The travel time of the SYSREF minus the travel time of DCLK needs to be less than 167 ps to meet the setup time and more than 0ps to meet the hold time. To roughly convert this travel time difference into inches we estimate the travel time through 1 inch of FR-4 material to be 167 ps per inch. So, for each SYSREF/DCLK pair in the system, the following routing requirement would need to be met:

DCLK trace length < SYSREF trace length < DCLK trace length + 1 inch

[2] Having the DLU requirement equal to the device clock is the worst case for meeting timing on SYSREF.

Meeting this requirement will ensure that the SYSREF transition will occur within the valid window as illustrated in Figure 4.

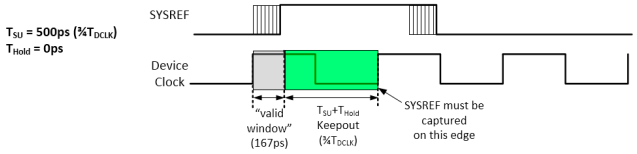


Figure 4. Meeting the SYSREF/DCLK Timing Requirement

INTERPAIR TRACE LENGTH MATCHING TO MEET DLU LIMIT

Since the DLU limit has been set to 667 ps and we know the relationship between the DLU limit and the interpair (or SYSREF) distribution skew (DS_{SYSREF}), it is a straightforward derivation to find the trace length match limit:

$$DS_{SYSREF} = DLU - T_{"Valid\ Window"}$$

$$= 667\ ps - 167\ ps = 500\ ps$$

So, the interpair distribution skew across all SYSREF/DCLK pairs must be within[3]:

$$500\ ps \div 167\ ps\ per\ inch = 3\ inches$$

Figure 5 illustrates the timing for this example. The "best case" distribution skew (DS_{SYSREF}) refers to the case that would allow for a less stringent trace length matching requirement.

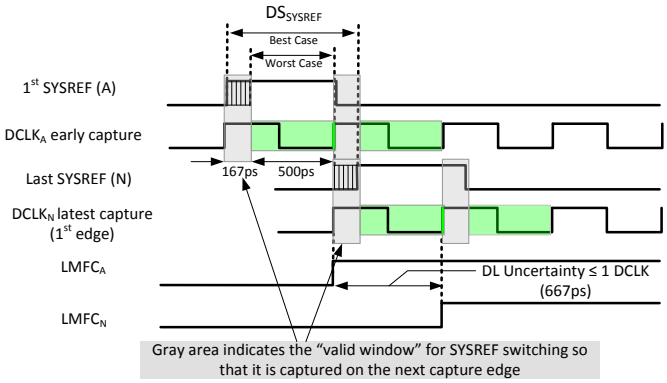


Figure 5. Meeting Interpair Distribution Skew Requirement

ADVANCED SOLUTIONS TO MEET SYSREF TIMING AND DLU LIMIT

Of course, the issue can be solved by using a slower device clock, which would make the length matching easier. This would come at the cost of sacrificing some system phase noise performance. A similar solution to this is to relax the DLU requirement, which would retain the advantage of the improved system phase noise performance. How the DLU requirement is established depends on the application. This will be discussed below in the context of deterministic latency accuracy. If the increased phase noise performance is required and the DLU requirement cannot be relaxed, it may prove too difficult to meet the routing requirement for SYSREF/DCLK intradevice skew and interdevice skew (1 inch and 3 inches, respectively, in the example above). In this case, adjustable phase delay for the device clock and/or SYSREF is required. The resolution of the adjustment must be less than the "valid window" based on the setup and hold time. From the example, the "valid window" is 167 ps.

Some FPGAs may have difficulty meeting small adjustment resolution requirements. However, the AD9528 meets this requirement since it is capable of adjusting SYSREF phase delay in 60 ps steps with less than 50 ps variability across all outputs. Figure 6 illustrates how SYSREF can be delayed to meet the timing requirements. In the illustration, SYSREF is delayed in 60 ps increments. Selecting a phase setting that places the SYSREF edge near the middle of the valid window is recommended. In the illustration, green edges indicate good phase settings and red edges indicate bad settings. The phase setting of 3 is in the middle of the valid window and should be used in this case.

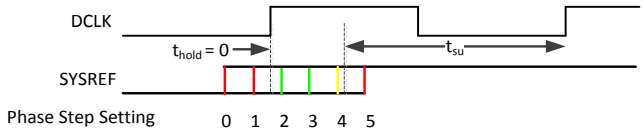


Figure 6. Programmable Phase Delay for SYSREF to Meet Timing

In addition to the 60 ps phase steps available on the SYSREF outputs, the AD9528's device clock outputs can be phase delayed by ½ of a device clock cycle. This feature is also helpful in meeting the SYSREF timing requirements.

2.2.3 SYSREF SETUP AND HOLD TIME MONITORING

ADI's AD9680 implements SYSEREF setup and hold time monitor circuits to help in the adjustment of the relative timing between SYSREF and device clock. By monitoring these two registers, the user is able to determine if there is a danger in violating the timing requirements for capturing SYSREF. If either of these registers give an indication that the timing margins are insufficient, the user knows he needs to adjust the relative position of SYSREF versus the device clock. This adjustment would be made in the above example by either adjusting the phase of SYSREF relative to device clock (using the AD9528, for example) or by adjusting the trace length of the SYSREF and/or device clock signal.

2.2.4 DETERMINISTIC LATENCY ACCURACY

To better understand how a system's deterministic latency uncertainty is set, an understanding of the application is required. Most systems requiring deterministic latency need to know exactly which sample in time marks the beginning

[3] 500 ps is the worst case skew for SYSREF and should be used to determine the trace length match limit.

of the data of interest. A common use for deterministic latency is for synchronizing multiple converters in a system. This is referred to as multichip synchronization. In these systems, sample alignment is needed across all converters. Therefore, deterministic latency must be "sample accurate." In these systems, the DLU needs to be ± ½ the sample clock. An advantage of having a device clock that is a multiple of the sample clock is that it simplifies the task of capturing SYSREF in such a way as to be sample accurate. In the AD9250 example, the device clock is 6 × the sample clock. In order to be sample accurate, the DLU requirements of ±½ the sample clock translates to be ±3 device clocks. This is illustrated Figure 7. Our example for the AD9250 showed that even the most stringent DLU requirement can be met easily with the ability to adjust the phase of the SYSREF at each device. When the device clock is a multiple of the sample clock, capturing SYSREF for sample accuracy is greatly simplified. As the sample rates for converters increase to 1 Gbps and beyond, the ability to phase delay the SYSREF and device clocks will become essential.

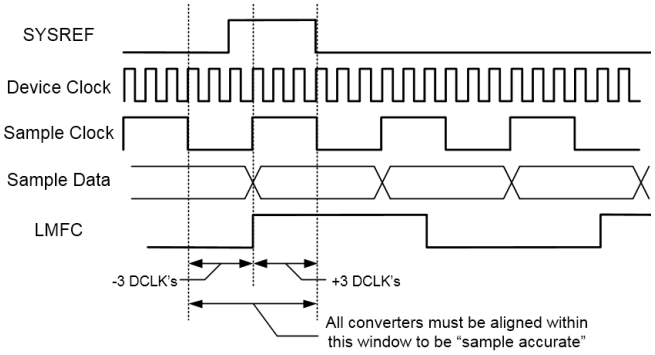


Figure 7. "Sample Accurate" Requirement for SYSREF Capture

2.3 POTENTIAL ISSUES WITH SYSREF CAPTURE

Other than meeting the SYSREF setup and hold time requirements and the DLU requirements, there are other potential issues that could occur related to SYSREF capture. For example, upon initial power-up of the system, it is possible that the SYSREF becomes active prior to the system clocks settling. This can happen when using a continuous SYSREF signal. This is resolved by including programmability in the JESD204B interface that allows the device to wait a certain number of edges before synchronizing clocks. Another programmability option could allow the user to "arm" the SYSREF capture when a valid edge is expected. This provides control over when to synchronize with a continuous SYSREF. Many ADI converter devices employing the JESD204B interface, including the AD9625 and AD9680, have these features.

Another example is that small variations in SYSREF may be able to cause an unnecessary resynchronization. This is resolved by including programmability in the JESD204B interface that allows the user to specify the valid window around the LMFC for the SYSREF edge. If the SYSREF occurs within this valid window, then the system is still considered to be "in-sync." This is a very useful feature since many applications monitor a continuous SYSREF signal to determine the state of the link. The LMFC boundary is compared to SYSREF to determine the state of synchronization in this case. ADI's AD9680 implements this feature as illustrated in Figure 8.

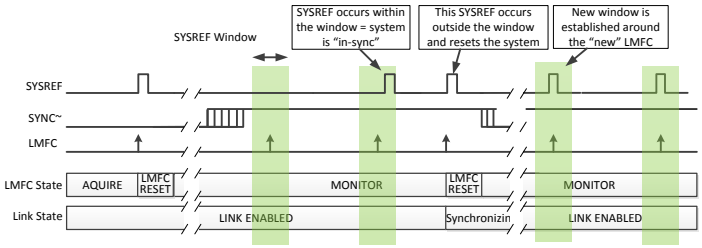


Figure 8. SYSREF Monitor Window

Other useful features for helping with SYSREF capture are the ability to change which edge of the device clock is used for SYSREF capture and which edge of SYSREF is used to align the LMFC. Many ADI converter devices employing the JESD204B interface include these features.

3 SUBCLASS 2

In a subclass 2 system, the accuracy of the deterministic latency depends on the timing relation between device clock and SYNC~ signals and a variety of items that will consume the timing budget that will be described forthcoming. As with subclass 1, the application's tolerance for deterministic latency uncertainty will be critical in defining the application's trace length matching requirements for SYNC~ and device clock.

3.1 CAPTURING AND LAUNCHING SYNC~ ACCURATELY

The challenge for meeting the timing requirements for capturing SYNC~ accurately is essentially the same challenge presented in the subclass 1 discussion on capturing SYSREF. However, since the clocking scheme in subclass 2 is system synchronous, you can no longer perform the timing analysis at each capture device independently from the others and it becomes increasingly difficult in a multiconverter application. Not only this, but you must also account for the uncertainty associated with the launching of the SYNC~ signal. Each device in a system that uses system synchronous clocking will consume a portion of the timing budget. Among the items consuming the timing budget are clock distribution skew (DS_{DCLK}), SYNC~ distribution skew ($DS_{SYNC\sim}$) for multiconverter systems, the propagation delay of the SYNC~ signal, setup and hold time requirement for

each JESD204B transmitter, and the clock-to-SYNC~ output delay at each JESD204B receiver's SYNC~ output.

3.2 UPPER LIMIT FOR DEVICE CLOCK IN SUBCLASS 2

The JESD204B standard acknowledges that a subclass 2 implementation will impose a limit on the device clock rate due to the system synchronous clocking scheme employed. Annex B in the standard suggests that this limit is 500 MHz:

"Since SYSREF is a source synchronous signal which can be generated in an accurate phase aligned manner with the device clock, it is expected that a system designer aiming to operate at device clock rates higher than 500 MHz would prefer to use a Subclass 1 approach."

Let's explore a detailed timing example in order to illustrate why such a limit exists.

A SUBCLASS 2 MULTIDAC TIMING EXAMPLE

Let's consider a transmitter application employing two subclass 2 DAC devices connected to a single logic device, as illustrated in Figure 9.

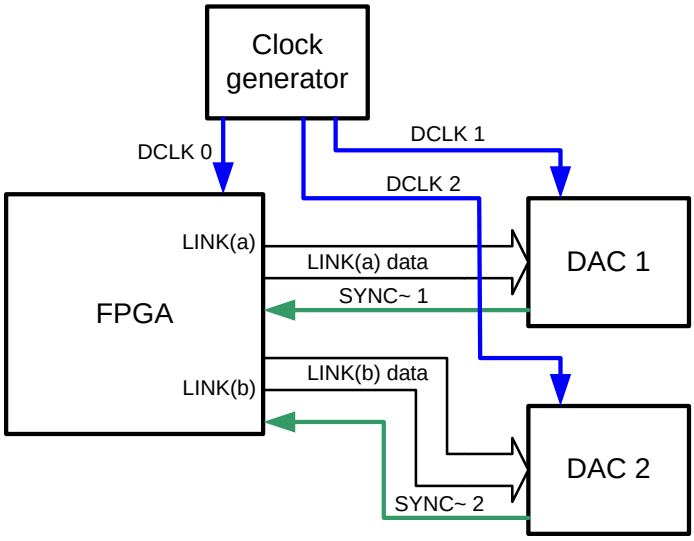


Figure 9. Subclass 2 MultiDAC Application

For the example, a 500 MHz device clock is used. The SYNC~ and DCLK signals have the PCB skews[4] listed below.

- Clock to FPGA = 300 ps
- Clock to DAC1 = 600 ps
- Clock to DAC2 = 720 ps
- SYNC~1 to FPGA = 660 ps
- SYNC~2 to FPGA = 750 ps

Before considering jitter and PVT variations, the timing is as illustrated in Figure 10. In the figure, the worst case timing is with the capture of the SYNC~2 signal at the FPGA input. The combination of DLCK2 propagation delay, SYNC~2 propagation delay, and clock-to-out delay of SYNC~2 leave 600 ps of setup time for capturing at the FPGA input.

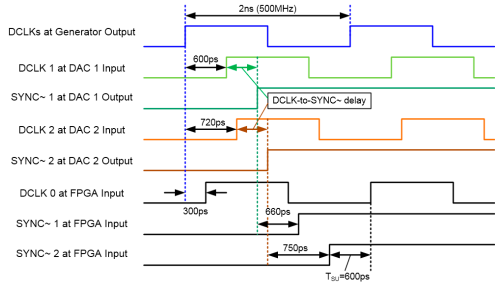


Figure 10. Subclass 2 MultiDAC Application SYNC~/DCLK Timing

However, once the setup time, jitter, and PVT variations are added, a timing violation can easily occur as illustrated in Figure 11. In the example, the setup time is 500 ps, the PVT variations[5] add up to 300 ps and jitter[6] is 150 ps. At the last arriving SYNC~ (SYNC~ 2), this creates a timing violation.

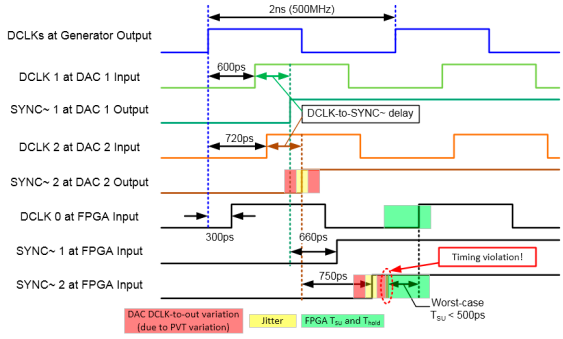


Figure 11. Subclass 2 MultiDAC Application SYNC~/DCLK Timing Violation

In the above example, trace length manipulation and/or clock phase adjustments can be made to resolve timing. However, as the frequency of DCLK increases, meeting the timing requirements becomes more difficult, even more than for subclass 1 implementation since more variables must be accounted for. Section 6.4 of the JESD204B standard covers the subject of SYNC~ capture timing in detail.

3.2.1 SUBCLASS 2 DETERMINISTIC LATENCY UNCERTAINTY

Just as with subclass 1, the timing constraints will be determined by the application's tolerance for deterministic latency uncertainty. Table 1 summarizes the variables that need to be accounted for when meeting subclass 2 timing requirements for a system's DLU.[7]

[4] 300 ps ≈ 1.8 inches of PCB trace.
[5] PVT variations at SYNC~ output and both clock outputs.
[6] Jitter on DLCK and SYNC~.
[7] In order to keep the illustration of the concept of DLU simple, clock jitter and variations due to process, voltage, and temperature (PVT) are not considered here.

Table 1. Timing variables affecting subclass 2 DLU

Application	Variable 1	Variable 2	Variable 3	Variable 4	Variable 5
Single converter	Clock-to-SYNC~ output delay	t_{SU} and t_{Hold} @ ADC	$T_{PD\_SYNC\sim}$	DS_{DCLK}	
Multiconverter	Clock-to-SYNC~ output delay	t_{SU} and t_{Hold} @ ADC	$T_{PD\_SYNC\sim}$	DS_{DCLK}	$DS_{SYNC\sim}$

DLU in a subclass 2 system is determined by the relationship between $T_{CLK\text{-}to\text{-}SYNC}$, $T_{PD\_SYNC\sim}$, and T_{SU} and the distribution skew of the device clocks (DS_{DCLK}) in the system. In a single converter application, the best case DLU is given by the following equation and is illustrated in Figure 12.

$$DLU = DS_{DCLK} = T_{CLK\text{-}to\text{-}SYNC} + T_{PD\_SYNC\sim} + T_{SU}$$

In the illustration, T_{SU} is ½ T_{DCLK} and T_{HOLD} is ¼ T_{DCLK}. As illustrated, the DLCK is skewed to match the DCLK-to-SYNC~ delay and SYNC~ propagation delay and just meet the setup time requirement.

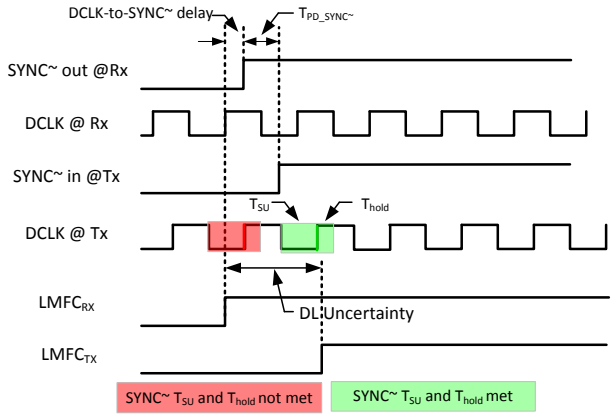


Figure 12. Subclass 2 SYNC~ Capture Timing for a Single Converter Application: Best Case DLU

The worst case DLU in a single converter subclass 2 system would occur when the DCLK at the transmitter is not skewed enough and violates the setup time of the first available capture edge, as illustrated in Figure 13.

$$DS_{DCLK} < T_{CLK\text{-}to\text{-}SYNC} + T_{SU} + T_{PD\_SYNC\sim}$$

$$DLU = T_{CLK\text{-}to\text{-}SYNC} + T_{PD\_SYNC\sim} + T_{SU} + T_{DCLK}$$

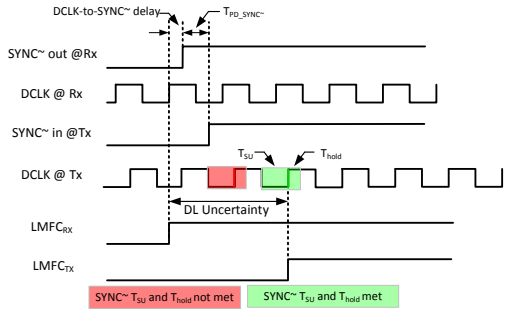


Figure 13. Subclass 2 SYNC~ Capture Timing for a Single Converter Application: Worst Case DLU

4 WHICH SUBCLASS IS BEST FOR YOUR APPLICATION?

Choosing which subclass to use for your JESD204B system depends on your need for deterministic latency, how accurate it needs to be if you need it, and the device clock requirements for your system.

Subclass 0 is easiest to implement and can be used when there is no need for deterministic latency. Even if your multiconverter system requires synchronization of the samples from all (or some) of the converters, this can be realized using the time stamp method supported by the AD9625 and AD9680.

Given the ability of subclass 1 to support ultrahigh device clock rates and that are used on high sample rate converters, it is the lowest risk solution for systems that require these high rates. Subclass 1 devices can be used at lower rates as well. If using a device clock rate below 500 MHz, meeting the timing requirements are fairly straightforward without having adjustability in the phase of the clock.

Subclass 2 devices can also be used below 500 MHz. The small advantage in using subclass 2 at lower rates is that it reduces the IO count on the logic device and eliminates the need to route SYSREF to each of the JESD204B devices.

RESOURCES

Share this article on

One Technology Way • P.O. Box 9106 • Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 • Fax: 781.461.3113 • www.analog.com

TA12595-0-7/14

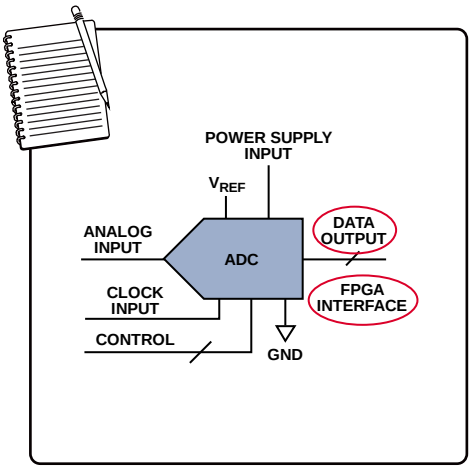
ANALOG DEVICES

Applications Engineering Notebook
MT-201

One Technology Way • P.O. Box 9106 • Norwood, MA 02062-9106, U.S.A. • Tel: 781.329.4700 • Fax: 781.461.3113 • www.analog.com

Interfacing FPGAs to an ADC Converter's Digital Data Output

by the Applications Engineering Group, Analog Devices, Inc.



The Applications Engineering Notebook Educational Series

IN THIS NOTEBOOK

Interfacing field programmable gate arrays (FPGAs) to analog-to-digital converter (ADC) output is a common engineering challenge. This notebook includes an overview of various interface protocols and standards as well as application tips and techniques for utilizing LVDS in high speed data converter implementations.

TABLE OF CONTENTS

REVISION HISTORY

1/13—Rev. 0 to Rev. A

Deleted Using Adapter Boards Section 11

1/12—Revision 0: Initial Version

INTERFACE STYLES AND STANDARDS

Interfacing field programmable gate arrays (FPGAs) to analog-to-digital converter (ADC) digital data output is a common engineering challenge. The task is complicated by the fact that ADCs use a variety of digital data styles and standards. Single data rate (SDR) CMOS is very common for lower speed data interfaces, typically under 200 MHz. In this case, data is transitioned on one edge of the clock by the transmitter and received by the receiver on the other clock edge. This ensures the data has plenty of time to settle before being sampled by the receiver. In double data rate (DDR) CMOS, the transmitter transitions data on every clock edge. This allows for twice as much data to be transferred in the same amount of time as SDR; however, the timing for proper sampling by the receiver is more complicated.

Parallel low voltage differential signaling (LVDS) is a common standard for high speed data converters. It uses differential signaling with a P and N wire for each bit to achieve speeds up to the range of 1.6 Gbps with DDR or 800 MHz in the latest FPGAs. Parallel LVDS consumes less power than CMOS, but requires twice the number of wires, which can make routing difficult. Though not part of the LVDS standard, LVDS is commonly used in data converters with a "source synchronous" clocking system. In this setup, a clock, which is in-phase with the data, is transmitted alongside the data. The receiver can then use this clock to capture the data easier, since it now knows the data transitions.

FPGA logic is often not fast enough to keep up with the bus speed of high speed converters, so most FPGAs have serializer/deserializer (SERDES) blocks to convert a fast, narrow serial interface on the converter side to a wide, slow parallel interface on the FPGA side. For each data bit in the bus, this block outputs 2, 4, or 8 bits, but at ½, ¼, or 1/8 the clock rate, effectively deserializing the data. The data is processed by wide busses inside the FPGA that run at much slower speeds than the narrow bus going to the converter.

The LVDS signaling standard is also used in serial links, mostly on high speed ADCs. Serial LVDS is typically used when pin count is more important than interface speed. Two clocks, the data rate clock and the frame clock, are often used. All the considerations mentioned in the parallel LVDS section also apply to serial LVDS. Parallel LVDS simply consists of multiple serial LVDS lines.

I^2C uses two wires: clock and data. It supports a large number of devices on the bus without additional pins. I^2C is relatively slow, 400 kHz to 1 MHz with protocol overhead. It is commonly used on slow devices where part size is a concern. I^2C is also often used as a control interface or data interface.

SPI uses 3 or 4 wires:

- Clock
- Data in and data out (4-wire), or bidirectional data in/data out (3-wire)
- Chip select (one per nonmaster device)

SPI supports as many devices as the number of available chip select lines. It provides speeds up to about 100 MHz and is commonly used as both a control interface and data interface.

Serial PORT (SPORT), a CMOS-based bidirectional interface, uses one or two data pins per direction. Its adjustable word length provides better efficiency for non %8 resolutions. SPORT offers time domain multiplexing (TDM) support and is commonly used on audio/media converters and high channel count converters. It offers performance of about 100 MHz per pin. SPORT is supported on Blackfin processors and offers straightforward implementation on FPGAs. SPORT is generally used for data only, although control characters can be inserted.

JESD204 is a JEDEC standard for high speed serial links between a single host, such as an FPGA or ASIC, and one or more data converters. The latest spec provides up to 3.125 Gbps per lane or differential pair. Future revisions may specify 6.25 Gbps and above. The lanes use 8B/10B encoding, reducing effective bandwidth of the lane to 80% of the theoretical value. The clock is embedded in data stream so there are no extra clock signals. Multiple lanes can be bonded together to increase throughput while the data link layer protocol ensures data integrity. JESD204 requires significantly more resources in FPGA/ASIC for data framing than simple LVDS or CMOS. It dramatically reduces wiring requirements at the expense of a more expensive FPGA and more sophisticated PCB routing.

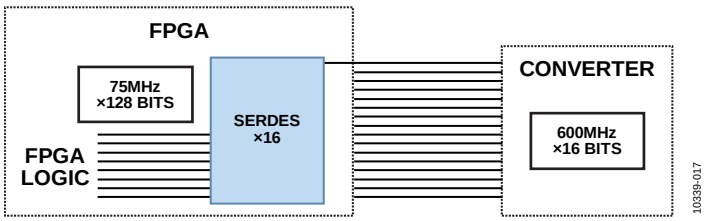


Figure 1. SERDES Blocks in FPGA Interface with High Speed Serial Interfaces on Converter

GENERAL RECOMMENDATIONS

Some general recommendations are helpful in interfacing between ADCs and FPGAs.

- Use external resistor terminations at the receiver, FPGA, or ASIC, rather than the internal FPGA terminations, to avoid reflections due to mismatch that can break the timing budget.
- Don't use one DCO from one ADC if you are using multiple ADCs in the system.
- Don't use a lot of "tromboning" when laying out digital traces to the receiver to keep all traces equal length.
- Use series terminations on CMOS outputs to slow edge rates down and limit switching noise. Verify that the right data format (twos complement, offset binary) is being used.

With single-ended CMOS digital signals, logic levels move at about 1 V/nS, typical output loading is 10 pF maximum, and typical charging currents are 10 mA/bit. Charging current should be minimized by using the smallest capacitive load possible. This can usually be accomplished by driving only one gate with the shortest trace possible, preferably without any vias. Charging current can also be minimized by using a damping resistor in digital outputs and inputs.

The time constant of the damping resistor and the capacitive load should be approximately 10% of the period of the sample rate. If the clock rate is 100 MHz and the loading is 10 pF, then the time constant should be 10% of 10 nS or 1 nS. In this case, R should be 100 Ω. For optimal signal-to-noise ratio (SNR) performance, a 1.8 V DRVDD is preferred over 3.3 V DRVDD. However, SNR is degraded when driving large capacitive loads. CMOS outputs are useable up to about 200 MHz sampling clocks. If driving two output loads or trace length is longer than 1 or 2 inches, a buffer is recommended.

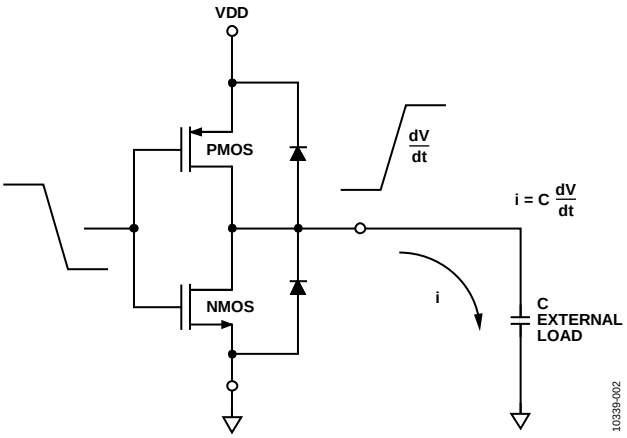


Figure 2. Typical CMOS Digital Output Drivers

ADC digital outputs should be treated with care because transient currents can increase the noise and distortion of the ADC by coupling back into the analog input.

Typical CMOS drivers shown in Figure 2 are capable of generating large transient currents, especially when driving capacitive loads. Particular care must be taken with CMOS data output ADCs so that these currents are minimized and do not generate additional noise and distortion in the ADC.

TYPICAL EXAMPLES

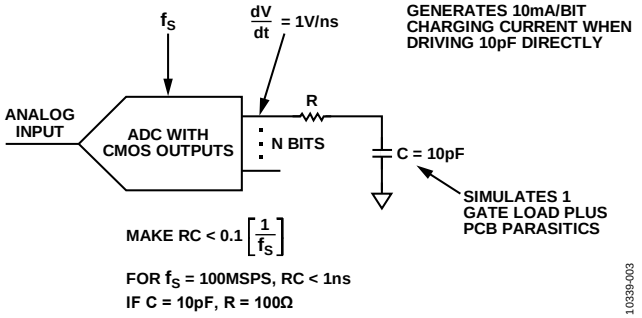


Figure 3. Use Series Resistance to Minimize Charging Current of CMOS Digital Outputs

Figure 3 shows the case of a 16-bit parallel CMOS output ADC. With a 10 pF load on each output, simulating one gate load plus PCB parasitics, each driver generates a charging current of 10 mA when driving a 10 pF load.

The total transient current for the 16-bit ADC can, therefore, be as high as 16 × 10 mA = 160 mA. These transient currents can be suppressed by adding a small resistor, R, in series with each data output. The value of the resistor should be chosen so that the RC time constant is less than 10% of the total sampling period. For *f*s = 100 MSPS, RC should be less than 1 ns. With C = 10 pF, an R of about 100 Ω is optimum. Choosing larger values of R can degrade output data settling time and interfere with proper data capture. Capacitive loading on CMOS ADC outputs should be limited to a single gate load, usually an external data capture register. Under no circumstances should the data output be connected directly to a noisy data bus. An intermediate buffer register must be used to minimize direct loading of the ADC outputs.

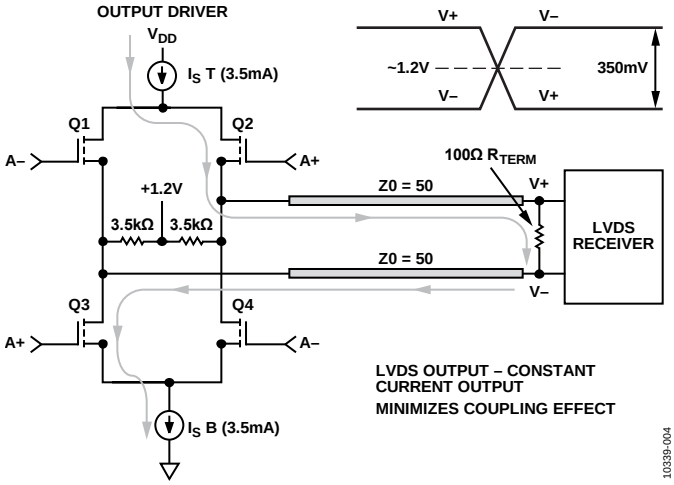


Figure 4. Typical LVDS Driver Design

Figure 4 shows a standard LVDS driver in CMOS. The nominal current is 3.5 mA and the common-mode voltage is 1.2 V. The swing on each input at the receiver is therefore 350 mV p-p when driving a 100 Ω differential termination resistor. This corresponds to a differential swing of 700 mV p-p. These figures are derived from the LVDS specification.

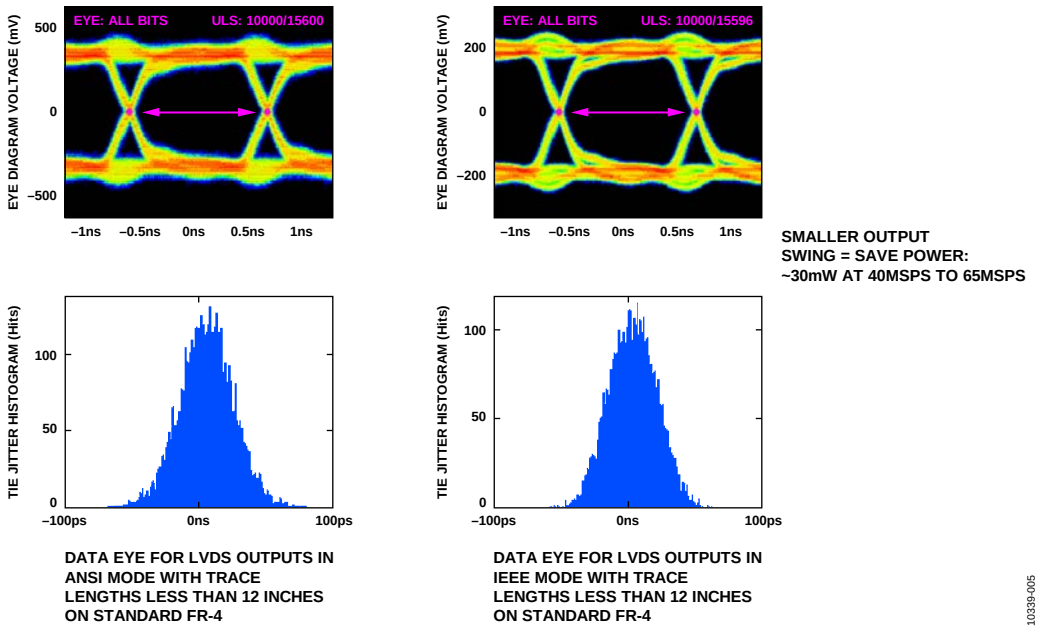


Figure 5. ANSI vs. IEEE LVDS Standards

There are two LVDS standards: one is defined by ANSI and the other by IEEE. While the two standards are similar and generally compatible with each other, they are not identical. Figure 5 compares an eye diagram and jitter histogram for each of the two standards. IEEE standard LVDS has a reduced swing of 200 mV p-p as compared to the ANSI standard of 320 mV p-p. This helps to save power on the digital outputs. For this reason, use the IEEE standard if it will accommodate the application and connections that need to be made to the receiver.

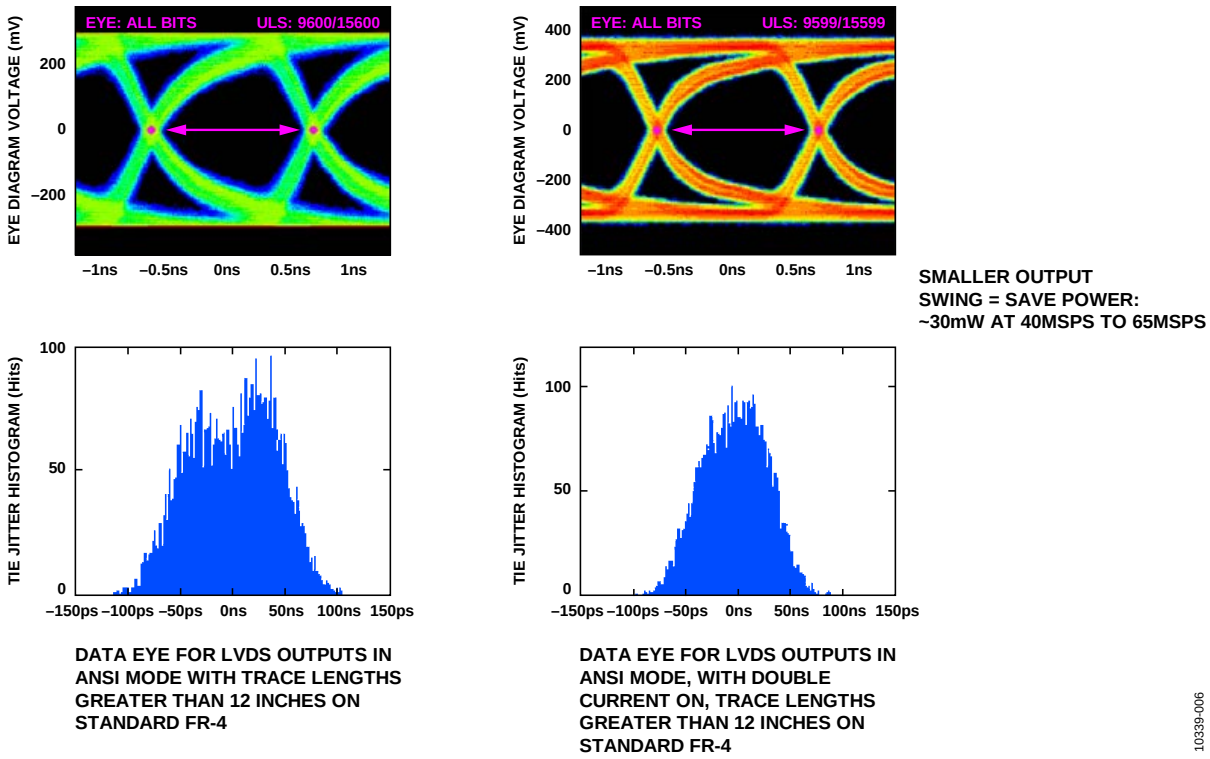


Figure 6. ANSI vs. IEEE LVDS Standards with Traces over 12 Inches

Figure 6 compares the ANSI and IEEE LVDS standards with long trace lengths above 12 inches or 30 cm. Both graphs are driven at the ANSI version standard. In the graph on the right, the output current is doubled. Doubling the output current cleans up the eye and improves the jitter histogram.

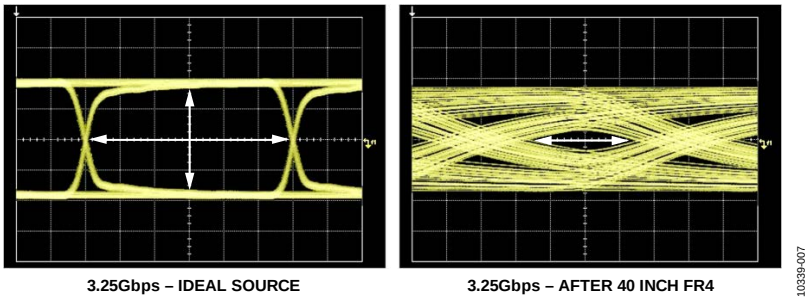


Figure 7. Effects of FR4 Channel Loss

Note the effects of a long trace on FR4 material in Figure 7. The left plot shows an ideal eye diagram, right at the transmitter. At the receiver, 40 inches away, the eye has almost closed and the receiver has difficulty recovering the data.

TROUBLESHOOTING TIPS

ADC WITH MISSING BIT 14

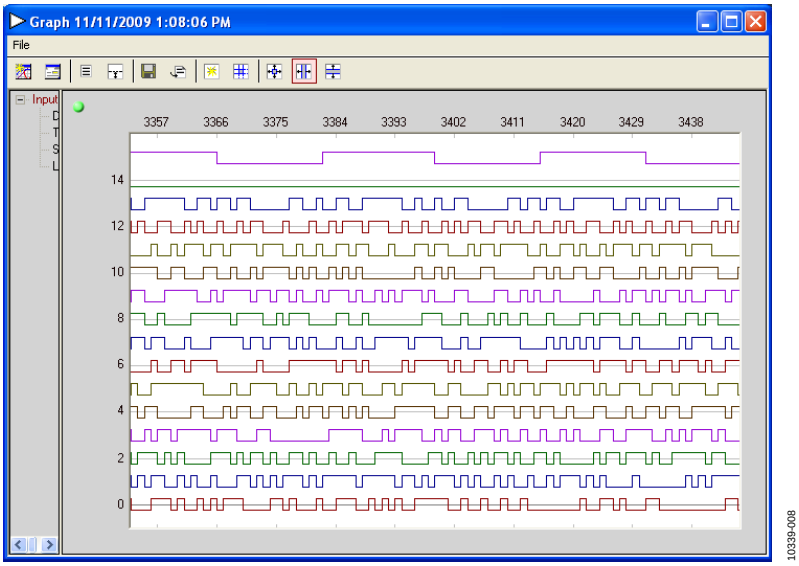


Figure 8. AD9268 ADC with Missing Bit 14

In Figure 8, a VisualAnalog digital display of the data bits shows that Bit 14 never toggles. This could indicate an issue with the part, the PCB, the receiver, or, that the unsigned data simply is not large enough to toggle the most significant bit.

ADC FREQUENCY DOMAIN PLOT WITH MISSING BIT 14

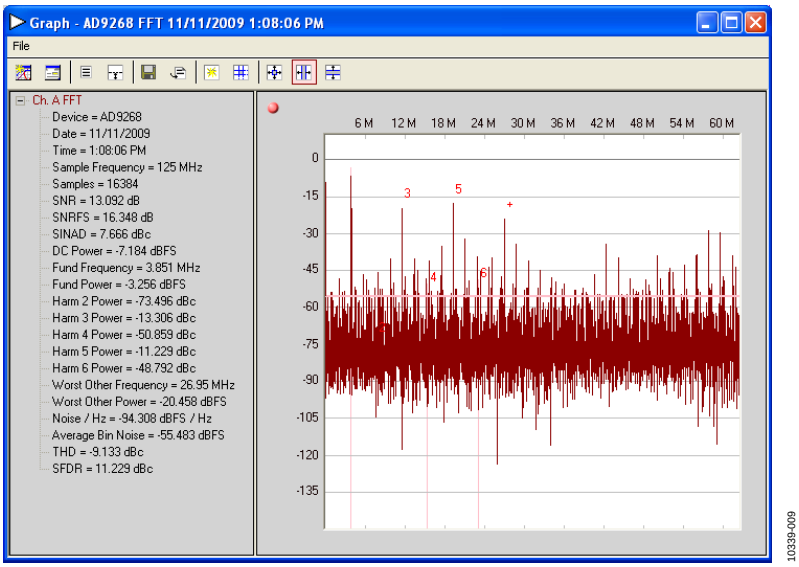


Figure 9. AD9268 ADC Frequency Domain Plot with Missing Bit 14

Figure 9 shows a frequency domain view of the previous digital data where Bit 14 is not toggling. The plot shows that the bit is significant and there is an error somewhere in the system.

ADC TIME DOMAIN PLOT WITH MISSING BIT 14

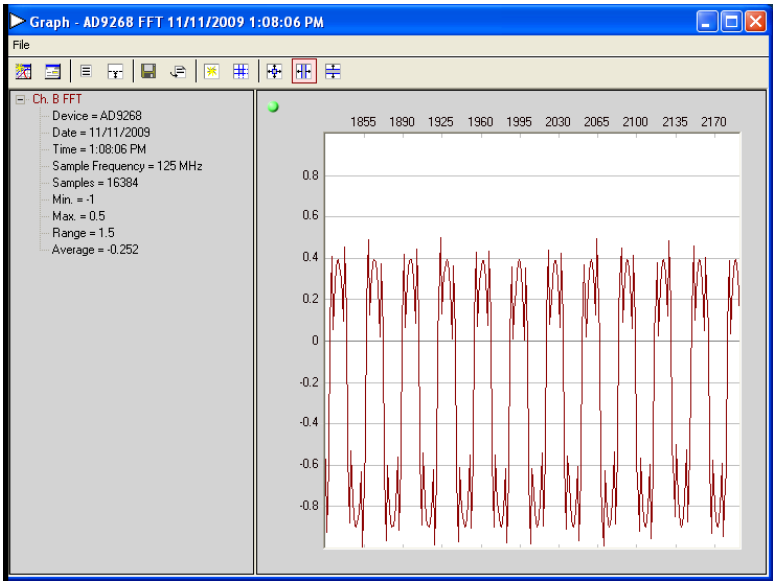


Figure 10. AD9268 ADC Time Domain Plot with Missing Bit 14

Figure 10 is a time domain plot of the same data. Instead of a smooth sine wave, the data is offset and has significant peaks at points throughout the waveform.

ADC WITH BIT 9 AND BIT 10 SHORTED TOGETHER

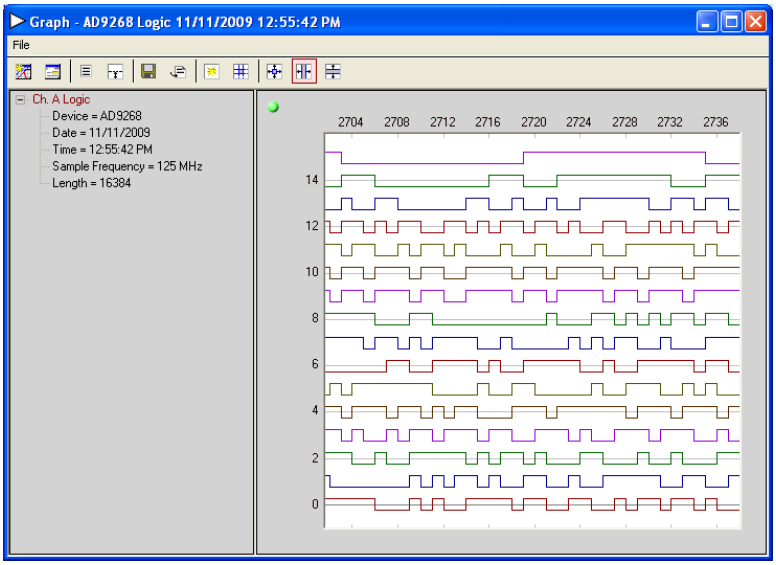


Figure 11. AD9268 ADC with Bit 9 and Bit 10 Shorted Together

In Figure 11, instead of missing a bit, two bits are shorted together so that the receiver always sees the same data on the two pins.

ADC FREQUENCY DOMAIN PLOT WITH BIT 9 AND BIT 10 SHORTED TOGETHER

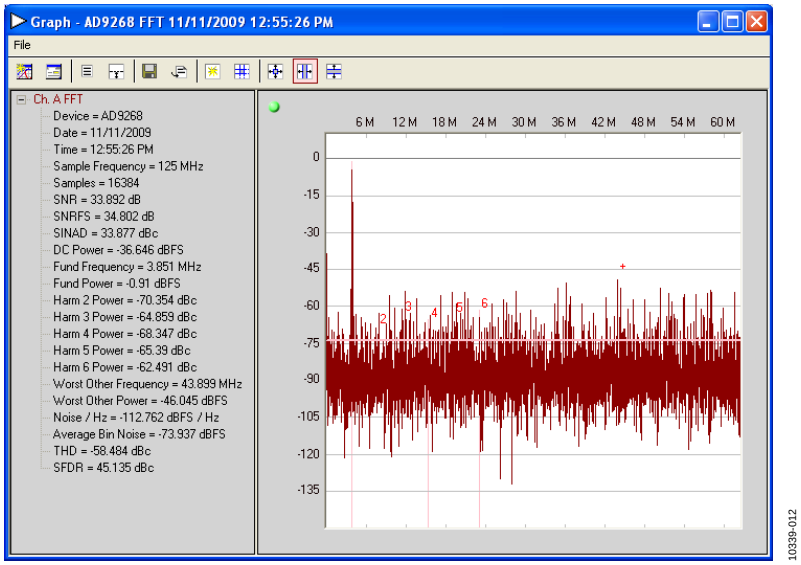


Figure 12. AD9268 ADC Frequency Domain Plot with Bit 9 and Bit 10 Shorted Together

Figure 12 shows a frequency domain view of the same case where two bits are shorted together. While the fundamental tone is clearly present, the noise floor is significantly worse than it should be. The degree to which the floor is distorted depends on which bits are shorted.

ADC TIME DOMAIN PLOT WITH BIT 9 AND BIT 10 SHORTED TOGETHER

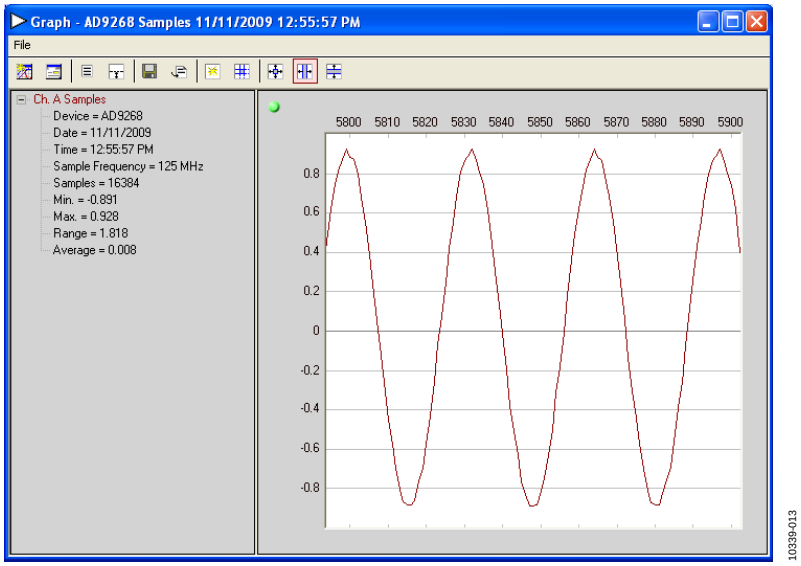


Figure 13. AD9268 ADC Time Domain Plot with Bit 9 and Bit 10 Shorted Together

In this time-domain view shown in Figure 13, the issue is less obvious. Although some smoothness is lost in the peaks and valleys of the wave, this is also common when the sample rate is close to the waveform's frequency.

TIME DOMAIN PLOT WITH INVALID DATA AND CLOCK TIMING

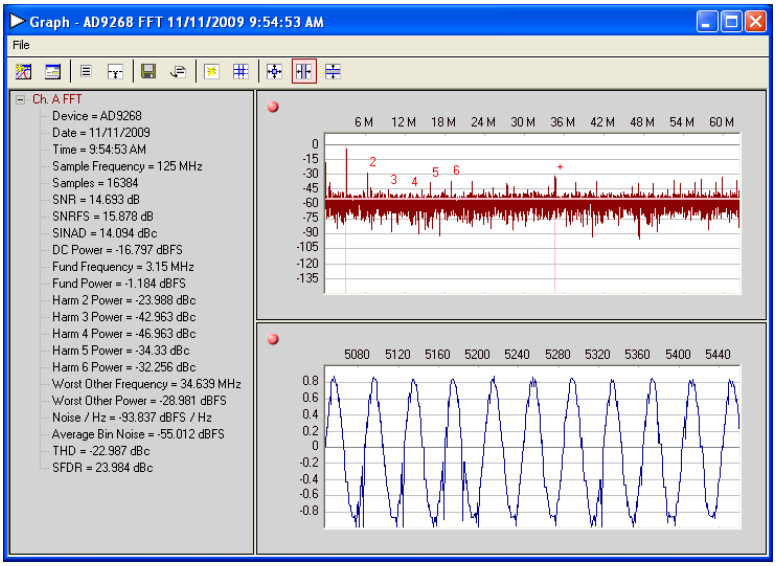


Figure 14. AD9268 Time Domain Plot with Invalid Data and Clock Timing

Figure 14 shows a converter with invalid timing, in this case caused by setup/hold problems. Unlike the previous errors, which generally showed themselves during each cycle of the data, timing errors are usually less consistent. Less severe timing errors may be intermittent. These plots show the time domain and frequency domain of a data capture that is not meeting timing. Notice that the errors in the time domain are not consistent between cycles. Also, note the elevated noise floor in the FFT/frequency domain. This usually indicates a missing bit, which can be caused by incorrect time alignment.

ZOOMED-IN TIME DOMAIN PLOT WITH INVALID DATA AND CLOCK TIMING

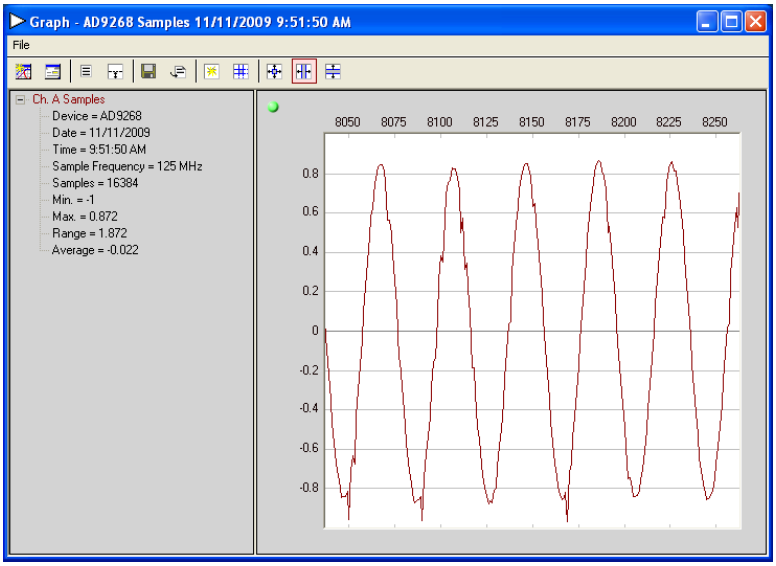


Figure 15. AD9268 Zoom-In Time Domain Plot with Invalid Data and Clock Timing

Figure 15 is a closer view of the time domain timing error shown in the Figure 14. Again, note that the errors are not consistent from cycle to cycle, but that certain errors do repeat. An example is the negative spike on the valley of several cycles in this plot.

MT10339-0-1/13(A)

Page 11 of 12 and Page 12 of 12 are blank.

Quad, 16-Bit, 2.8 GSPS, TxDAC+® Digital-to-Analog Converter

Data Sheet **AD9144**

FEATURES

- Supports input data rate >1 GSPS
- Proprietary low spurious and distortion design
  - 6-carrier GSM IMD = 77 dBc at 75 MHz IF
  - SFDR = 82 dBc at dc IF, −9 dBFS
  - Flexible 8-lane JESD204B interface
  - Support quad or dual DAC mode at 2.8 GSPS
- Multiple chip synchronization
  - Fixed latency
  - Data generator latency compensation
- Selectable 1×, 2×, 4×, 8× interpolation filter
  - Low power architecture
- Input signal power detection
  - Emergency stop for downstream analog circuitry protection
- Transmit enable function allows extra power saving
- High performance, low noise phase-locked loop (PLL) clock multiplier
- Digital inverse sinc filter
- Low power: 1.6 W at 1.6 GSPS, 1.7 W at 2.0 GSPS, full operating conditions
- 88-lead LFCSP with exposed pad

APPLICATIONS

- Wireless communications
  - 3G/4G W-CDMA base stations
  - Wideband repeaters
  - Software defined radios
- Wideband communications
  - Point-to-point
  - Local multipoint distribution service (LMDS) and multichannel multipoint distribution service (MMDS)
- Transmit diversity, multiple input/multiple output (MIMO)
- Instrumentation
- Automated test equipment

GENERAL DESCRIPTION

The AD9144 is a quad, 16-bit, high dynamic range digital-to-analog converter (DAC) that provides a maximum sample rate of 2.8 GSPS, permitting a multicarrier generation up to the Nyquist frequency. The DAC outputs are optimized to interface seamlessly with the ADRF672x analog quadrature modulators (AQMs) from Analog Devices, Inc. An optional 3-wire or 4-wire serial port interface (SPI) provides for programming/readback of many internal parameters. Full-scale output current can be programmed over a typical range of 13.9 mA to 27.0 mA. The AD9144 is available in an 88-lead LFCSP.

FUNCTIONAL BLOCK DIAGRAM

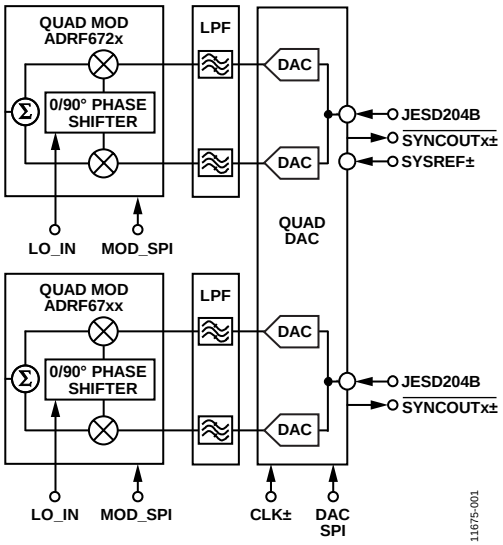


Figure 1.

PRODUCT HIGHLIGHTS

1. Greater than 1 GHz, ultrawide complex signal bandwidth enables emerging wideband and multiband wireless applications.
2. Advanced low spurious and distortion design techniques provide high quality synthesis of wideband signals from baseband to high intermediate frequencies.
3. JESD204B Subclass 1 support simplifies multichip synchronization in software and hardware design.
4. Fewer pins for data interface width with a serializer/deserializer (SERDES) JESD204B eight-lane interface.
5. Programmable transmit enable function allows easy design balance between power consumption and wake-up time.
6. Small package size with 12 mm × 12 mm footprint.

Rev. 0 Document Feedback

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700
Technical Support www.analog.com

12-Bit, 1 GSPS JESD204B, Dual Analog-to-Digital Converter

Data Sheet **AD9234**

FEATURES

- JESD204B (Subclass 1) coded serial digital outputs
- 1.5 W total power per channel at 1 GSPS (default settings)
- SFDR = 79 dBFS at 340 MHz
- SNR = 63.4 dBFS at 340 MHz (A_{IN} = −1.0 dBFS)
- ENOB = 10.4 bits at 10 MHz
- DNL = ±0.16 LSB
- INL = ±0.35 LSB
- Noise density = −151 dBFS/Hz at 1 GSPS
- 1.25 V, 2.5 V, and 3.3 V dc supply operation
- No missing codes
- Internal ADC voltage reference
- Flexible termination impedance
  - 400 Ω, 200 Ω, 100 Ω, and 50 Ω differential
- 2 GHz usable analog input full power bandwidth
- 95 dB channel isolation/crosstalk
- Amplitude detect bits for efficient AGC implementation
- Differential clock input
- Optional decimate-by-2 DDC per channel
- Differential clock input
- Integer clock divide by 1, 2, 4, or 8
- Flexible JESD204B lane configurations
- Small signal dither

APPLICATIONS

- Communications
- Diversity multiband, multimode digital receivers
  - 3G/4G, TD-SCDMA, W-CDMA, GSM, LTE
- Point-to-point radio systems
- Digital predistortion observation path
- General-purpose software radios
- Ultrawideband satellite receiver
- Instrumentation (spectrum analyzers, network analyzers, integrated RF test solutions)
- Digital oscilloscopes
- High speed data acquisition systems
- DOCSIS 3.0 CMTS upstream receive paths
- HFC digital reverse path receivers

FUNCTIONAL BLOCK DIAGRAM

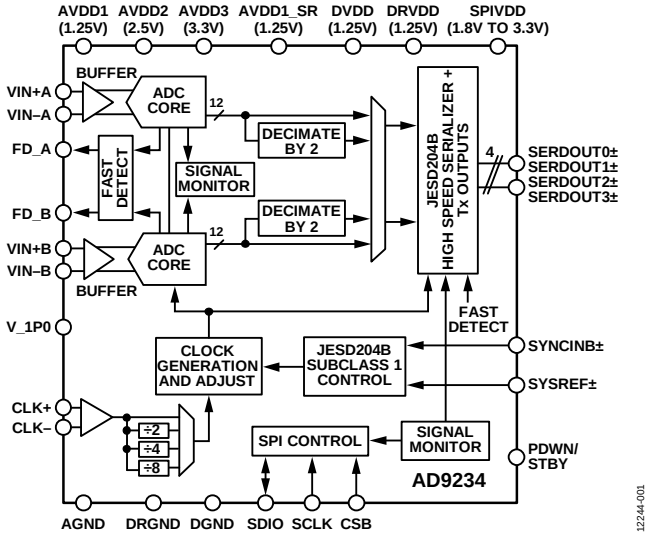


Figure 1.

PRODUCT HIGHLIGHTS

1. Low power consumption analog core, 12-bit, 1.0 GSPS dual analog-to-digital converter (ADC) with 1.5 W per channel.
2. Wide full power bandwidth supports IF sampling of signals up to 2 GHz.
3. Buffered inputs with programmable input termination eases filter design and implementation.
4. Flexible serial port interface (SPI) controls various product features and functions to meet specific system requirements.
5. Programmable fast overrange detection.
6. 9 mm × 9 mm 64-lead LFCSP.
7. Pin compatible with the AD9680 14-bit, 1 GSPS dual ADC.

Rev. 0 Document Feedback

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 ©2014 Analog Devices, Inc. All rights reserved.
Technical Support www.analog.com

14-Bit, 170 MSPS/250 MSPS, JESD204B, Dual Analog-to-Digital Converter

Data Sheet **AD9250**

FEATURES

- JESD204B Subclass 0 or Subclass 1 coded serial digital outputs
- Signal-to-noise ratio (SNR) = 70.6 dBFS at 185 MHz AIN and 250 MSPS
- Spurious-free dynamic range (SFDR) = 88 dBc at 185 MHz AIN and 250 MSPS
- Total power consumption: 711 mW at 250 MSPS
- 1.8 V supply voltages
- Integer 1-to-8 input clock divider
- Sample rates of up to 250 MSPS
- IF sampling frequencies of up to 400 MHz
- Internal analog-to-digital converter (ADC) voltage reference
- Flexible analog input range
  - 1.4 V p-p to 2.0 V p-p (1.75 V p-p nominal)
- ADC clock duty cycle stabilizer (DCS)
- 95 dB channel isolation/crosstalk
- Serial port control
- Energy saving power-down modes

FUNCTIONAL BLOCK DIAGRAM

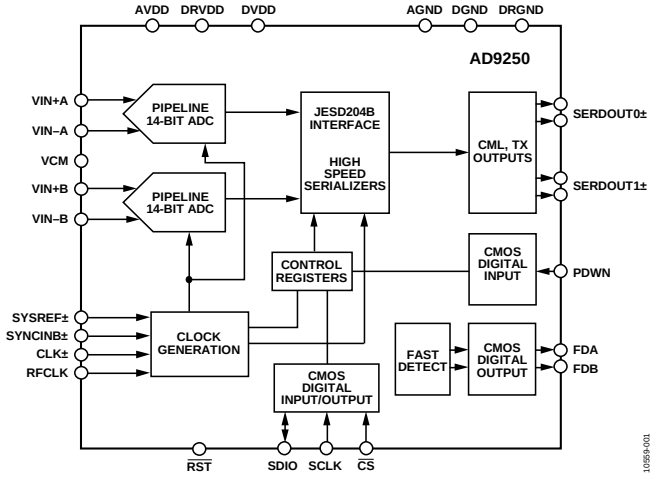


Figure 1.

APPLICATIONS

- Diversity radio systems
- Multimode digital receivers (3G)
  - TD-SCDMA, WiMAX, WCDMA, CDMA2000, GSM, EDGE, LTE
- DOCSIS 3.0 CMTS upstream receive paths
- HFC digital reverse path receivers
- I/Q demodulation systems
- Smart antenna systems
- Electronic test and measurement equipment
- Radar receivers
- COMSEC radio architectures
- IED detection/jamming systems
- General-purpose software radios
- Broadband data applications

PRODUCT HIGHLIGHTS

1. Integrated dual, 14-bit, 170 MSPS/250 MSPS ADC.
2. The configurable JESD204B output block supports up to 5 Gbps per lane.
3. An on-chip, phase-locked loop (PLL) allows users to provide a single ADC sampling clock; the PLL multiplies the ADC sampling clock to produce the corresponding JESD204B data rate clock.
4. Support for an optional RF clock input to ease system board design.
5. Proprietary differential input maintains excellent SNR performance for input frequencies of up to 400 MHz.
6. Operation from a single 1.8 V power supply.
7. Standard serial port interface (SPI) that supports various product features and functions such as controlling the clock DCS, power-down, test modes, voltage reference mode, over range fast detection, and serial output configuration.

Rev. B Document Feedback

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700
Technical Support www.analog.com

12-Bit, 2.5/2.0 GSPS, 1.3 V/2.5 V Analog-to-Digital Converter

Preliminary Data Sheet

AD9625

FEATURES

12-bit 2.5 GSPS ADC, no missing codes
SFDR = 79dBc, AIN up to 1 GHz at −1 dBFS, 2.5 GSPS
SFDR = 75dBc, AIN up to 1.8 GHz at −1 dBFS, 2.5 GSPS
SNR = 57.6 dBFS, AIN up to 1 GHz at −1 dBFS, 2.5 GSPS
SNR = 56.7 dBFS, AIN up to 1.8 GHz at −1 dBFS, 2.5 GSPS
Noise Spectral Density = −150 dBFS/Hz at 2.5 GSPS
Power consumption: 3.8W at 2.5 GSPS
Differential analog input: 1.1 Vp-p
Differential clock input
High speed 6- or 8-lane JESD204B serial output
Subclass 1: 6.25 Gbps at 2.5 GSPS
Two independent decimate by 8 or decimate by 16 filters with 10-bit NCOs
Supply voltages: 1.3 V, 2.5 V
Serial port control
Flexible digital output modes
Built-in selectable digital test patterns

APPLICATIONS

Spectrum analyzers
Military communications
Radar
High performance digital storage oscilloscopes
Active jamming/antijamming
Electronic surveillance and countermeasures

FUNCTIONAL BLOCK DIAGRAM

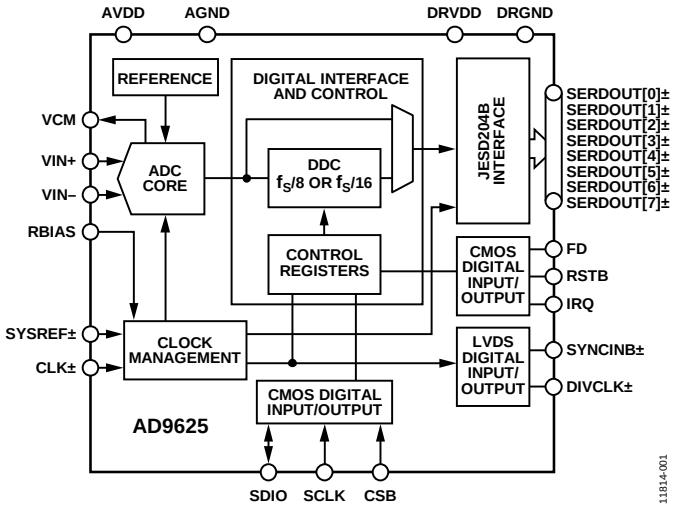


Figure 1.

GENERAL DESCRIPTION

The AD9625 is a 12-bit monolithic sampling analog-to-digital converter (ADC) that operates at conversion rates of up to 2.5 giga samples per second (GSPS). This product is designed for sampling wide bandwidth analog signals up to the second Nyquist zone. The combination of wide input bandwidth, high sampling rate, and excellent linearity of the AD9625 is ideally suited for spectrum analyzers, data acquisition systems, and a wide assortment of military electronics applications, such as radar and jamming/antijamming measures.

The analog input, clock, and SYSREF± signals are differential inputs. The JESD204B-based high speed serialized output is configurable in a variety of one-, two-, four-, six-, or eight-lane configurations. The product is specified over the industrial temperature range of −40°C to +85°C.

PRODUCT HIGHLIGHTS

1. High performance: exceptional SFDR in high sample rate applications, direct RF sampling, and on-chip reference.
2. Flexible digital data output formats based on the JESD204B specification.
3. Control path SPI interface port that supports various product features and functions, such as data formatting, gain, and offset calibration values.

Rev. Pr. A **Document Feedback**

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700
Technical Support www.analog.com

Octal Ultrasound AFE With JESD204B

Data Sheet **AD9675**

FEATURES

- 8 channels of LNA, VGA, AAF, ADC, and digital RF decimator
  - Low power: 150 mW per channel, TGC mode, 40 MSPS;
    62.5 mW per channel, CW mode; <30 mW at power-up
  - 10 mm × 10 mm, 144-ball CSP_BGA
  - TGC channel input referred noise: 0.82 nV/√Hz, maximum gain
  - Flexible power-down modes
  - Fast recovery from low power standby mode: 2 µs
- Low noise preamplifier (LNA)
  - Input-referred noise: 0.78 nV/√Hz, gain = 21.6 dB
  - Programmable gain: 15.6 dB/17.9 dB/21.6 dB
  - 0.1 dB compression: 1000 mV p-p/750 mV p-p/450 mV p-p
  - Flexible active input impedance matching
- Variable gain amplifier (VGA)
  - Attenuator range: 45 dB, linear-in-dB gain control
  - Postamp gain (PGA): 21 dB/24 dB/27 dB/30 dB
- Antialiasing filter (AAF)
  - Programmable second-order low-pass filter (LPF) from 8 MHz to 18 MHz or 13.5 MHz to 30 MHz and high-pass filter (HPF)
- Analog-to-digital converter (ADC)
  - SNR: 75 dB, 14 bits up to 125 MSPS
- JESD204B Subclass 0 coded serial digital outputs
- CW Doppler mode harmonic rejection I/Q demodulator
  - Individual programmable phase rotation
  - Dynamic range per channel: 160 dBFS/√Hz
  - Close-in SNR: 156 dBc/√Hz, 1 kHz offset, −3 dBFS
- RF digital decimation by 2 and high-pass filter

GENERAL DESCRIPTION

The AD9675 is designed for low cost, low power, small size, and ease of use for medical ultrasound. It contains eight channels of a variable gain amplifier (VGA) with a low noise preamplifier (LNA), a continuous wave (CW) harmonic rejection I/Q demodulator with programmable phase rotation, an antialiasing filter (AAF), an analog-to-digital converter (ADC), and a digital high-pass filter and RF decimation by 2 for data processing and bandwidth reduction.

Each channel features a maximum gain of up to 52 dB, a fully differential signal path, and an active input preamplifier termination. The channel is optimized for high dynamic performance and low power in applications where a small package size is critical.

The LNA has a single-ended-to-differential gain that is selectable through the SPI. Assuming a 15 MHz noise bandwidth (NBW) and a 21.6 dB LNA gain, the LNA input SNR is 94 dB. In CW Doppler mode, each LNA output drives an I/Q demodulator that has independently programmable phase rotation with 16 phase settings.

Power-down of individual channels is supported to increase battery life for portable applications. Standby mode allows quick power-up for power cycling. In CW Doppler operation, the VGA, AAF, and ADC are powered down. The ADC contains several features designed to maximize flexibility and minimize system cost, such as a programmable clock, data alignment, and programmable digital test pattern generation. The digital test patterns include built-in fixed patterns, built-in pseudorandom patterns, and custom user-defined test patterns entered via the serial port interface. This product is protected by a U.S. patent.

FUNCTIONAL BLOCK DIAGRAM

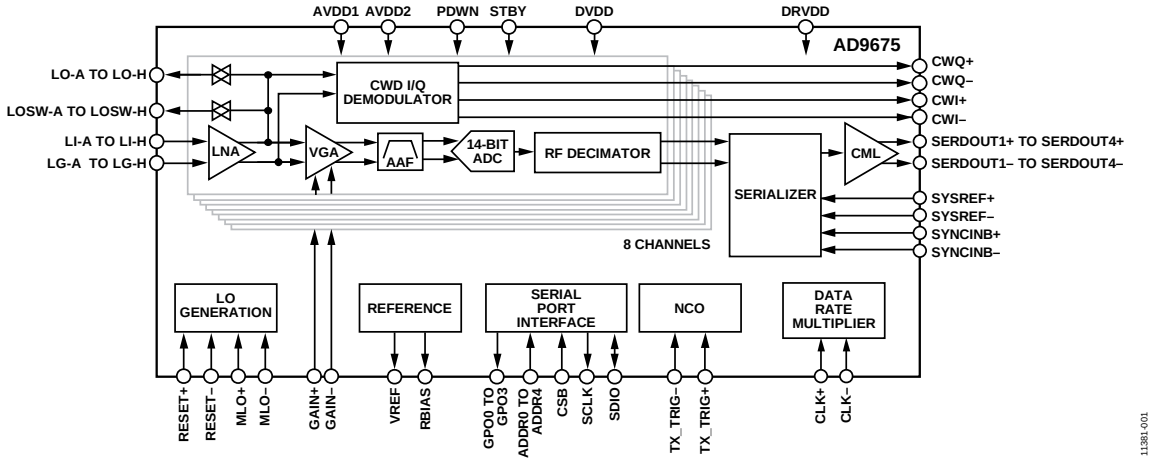


Figure 1.

For more information about the AD9675, contact Analog Devices, Inc., at Highspeed.converters@analog.com.

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700

Technical Support www.analog.com

14-Bit, 1 GSPS JESD204B, Dual Analog-to-Digital Converter

Data Sheet **AD9680**

FEATURES

- JESD204B (Subclass 1) coded serial digital outputs
- 1.65 W total power per channel at 1 GSPS (default settings)
- SFDR = 85 dBFS at 340 MHz, 80 dBFS at 1 GHz
- SNR = 65.3 dBFS at 340 MHz (A_{IN} = −1.0 dBFS),
  - 61.4 dBFS at 1 GHz
- ENOB = 10.8 bits at 10 MHz
- DNL = ±0.5 LSB
- INL = ±2.5 LSB
- Noise density = −154 dBFS/Hz at 1 GSPS
- 1.25 V, 2.5 V, and 3.3 V dc supply operation
- No missing codes
- Internal ADC voltage reference
- Flexible input range and termination impedance
  - 1.46 V p-p to 1.94 V p-p (1.70 V p-p nominal)
  - 400 Ω, 200 Ω, 100 Ω, and 50 Ω differential
- 2 GHz usable analog input full power bandwidth
- 95 dB channel isolation/crosstalk
- Amplitude detect bits for efficient AGC implementation
- 2 integrated wideband digital processors per channel
  - 12-bit NCO, up to 4 cascaded half-band filters
- Differential clock input
- Integer clock divide by −1, 2, 4, or 8
- Flexible JESD204B lane configurations
- Small signal dither

APPLICATIONS

- Communications
- Diversity multiband, multimode digital receivers
  - 3G/4G, TD-SCDMA, W-CDMA, GSM, LTE
- General-purpose software radios
- Ultrawideband satellite receivers
- Instrumentation
- Radars
- Signals intelligence (SIGINT)
- DOCSIS 3.0 CMTS upstream receive paths
- HFC digital reverse path receivers

FUNCTIONAL BLOCK DIAGRAM

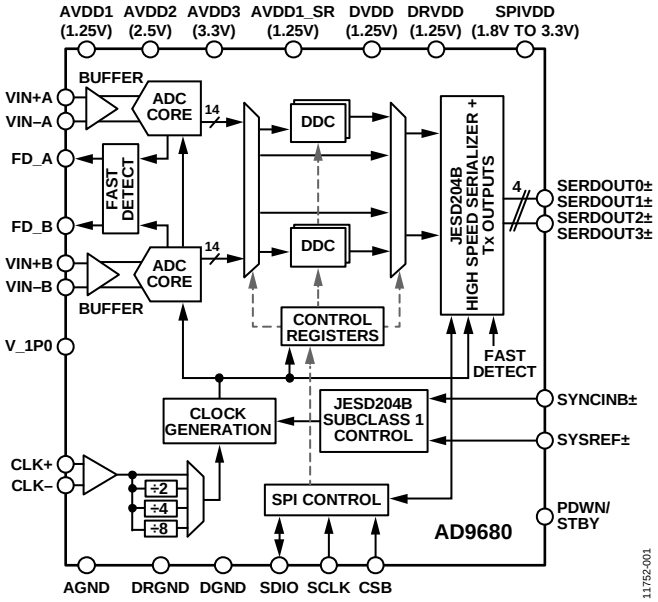


Figure 1.

PRODUCT HIGHLIGHTS

1. Wide full power bandwidth supports IF sampling of signals up to 2 GHz.
2. Buffered inputs with programmable input termination eases filter design and implementation.
3. Four integrated wideband decimation filters and numerically controlled oscillator (NCO) blocks supporting multiband receivers.
4. Flexible serial port interface (SPI) controls various product features and functions to meet specific system requirements.
5. Programmable fast overrange detection.
6. 9 mm × 9 mm 64-lead LFCSP.

Rev. 0 Document Feedback

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 ©2014 Analog Devices, Inc. All rights reserved.
Technical Support www.analog.com

More JESD204 Information

Useful Links

www.jedec.org

www.analog.com/JESD204

www.xilinx.com/products/intellectual-property/EF-DI-JESD204.htm

www.planetanalog.com/author.asp?section_id=3041&doc_id=561117&

www.electronicdesign.com/analog/pair-right-jesd204b-converter-your-fpga

www.eetimes.com/document.asp?doc_id=1280943

www.electronicdesign.com/analog/kickstart-your-system-designs-jesd204b

Videos

Rapid Prototyping with JESD204B Using FMC and Xilinx FPGAs

A Look at the JESD204B Serial Interface EYE Diagram

Analog Devices, Inc.
Worldwide Headquarters
Analog Devices, Inc.
One Technology Way
P.O. Box 9106
Norwood, MA 02062-9106
U.S.A.
Tel: 781.329.4700
(800.262.5643,
U.S.A. only)
Fax: 781.461.3113

Analog Devices, Inc.
Europe Headquarters
Analog Devices, Inc.
Wilhelm-Wagenfeld-Str. 6
80807 Munich
Germany
Tel: 49.89.76903.0
Fax: 49.89.76903.157

Analog Devices, Inc.
Japan Headquarters
Analog Devices, KK
New Pier Takeshiba
South Tower Building
1-16-1 Kaigan, Minato-ku,
Tokyo, 105-6891
Japan
Tel: 813.5402.8200
Fax: 813.5402.1064

Analog Devices, Inc.
Asia Pacific Headquarters
Analog Devices
5F, Sandhill Plaza
2290 Zuchongzhi Road
Zhangjiang Hi-Tech Park
Pudong New District
Shanghai, China 201203
Tel: 86.21.2320.8000
Fax: 86.21.2320.8222

G11313-0-8/14(C)

www.analog.com

ANALOG DEVICES