# Linearization DesignGuide Reference

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The following sections provide reference information on the use of the Linearization DesignGuide.

## Using the Linearization DesignGuide

The Linearization DesignGuide is integrated into Agilent EEsof's Advanced Design System environment. It contains many templates to be used within ADS. These templates can assist developers in designing a linearizer to meet performance specifications. This Design Guide provides a complete tool kit to interactively explore dynamic linearization systems at the top level as part of an integrated design process.

In addition to the requirements of the ADS software, the Linearization DesignGuide will require approximately 30 MB of additional storage space.

Note

This documentation assumes that you are familiar with all of the basic ADS program operations. For additional information, refer to Schematic Capture and Layout.

The primary features of this DesignGuide include the following:

- Complete linearization capability
- FeedForward (8-step design process)
- FeedForward (IS-95, CDMA2000, pi/4 DQPSK and 16 QAM simulation)
- RF predistortion (7-step design process)
- RF predistortion (IS-95 CDMA, pi/4 DQPSK and 16 QAM simulation)
- FeedForward combined with RF predistortion (10-step design process)
- Analog Predistortion (3-step design process for Cubic Law)
- Analog Predistortion (3-step design process for Square Law)
- LINC design (5-step design process)
- LINC design (IS-95 CDMA, pi/4 DQPSK and 16 QAM simulation)
- Cartesian feedback (2-step design process)
- Cartesian feedback (IS-95 CDMA, pi/4 DQPSK and 16 QAM simulation)
- Digital predistortion (6-step design process)
- Digital predistortion (IS-95, CDMA2000, pi/4 DQPSK and 16 QAM simulation)
- Memory Effects (Short Time Constant simulation)
- Memory Effects (Long Time Constant: IS-95, CDMA2000 and pi/4 DQPSK simulations)
- Digital Predistortion with Memory Effects (technique using ADS/ESG/VSA/Matlab)
- Crest Factor Reduction

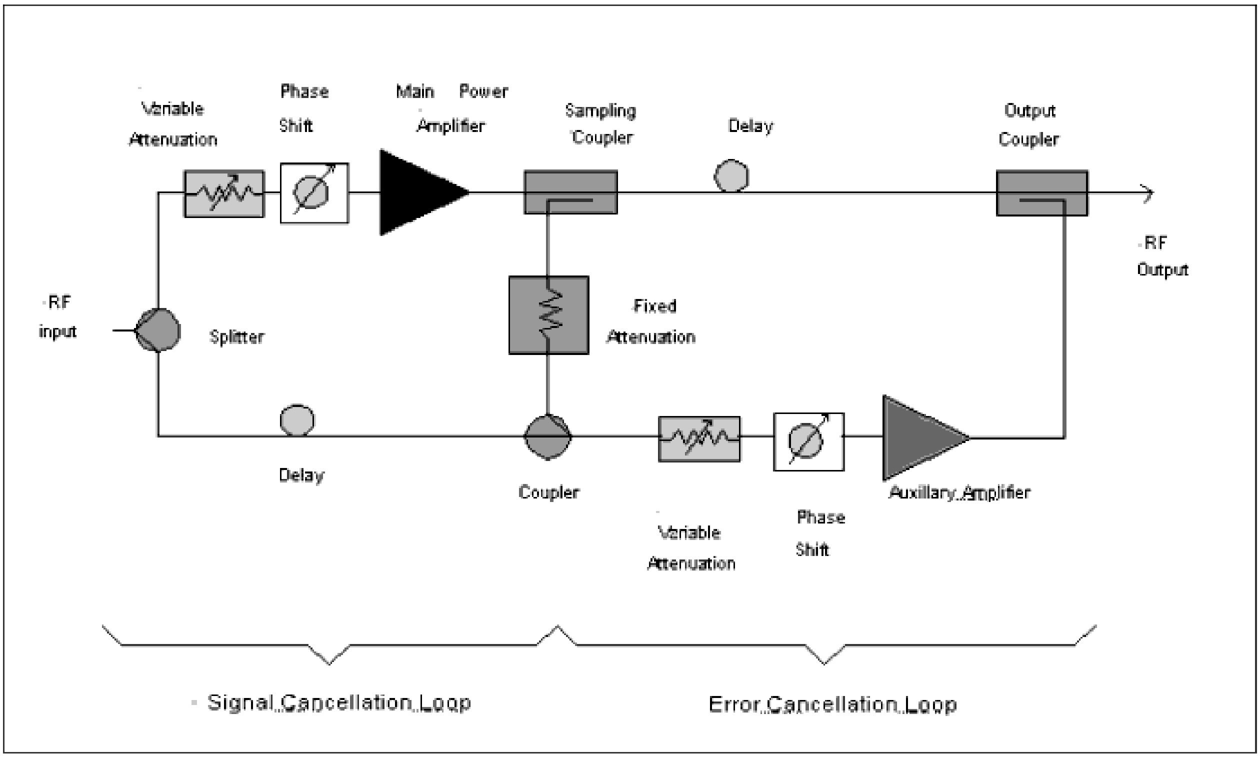
- ACPR optimization technique
- Gradient optimization technique
- Distinct ADS Ptolemy demos
- Feedforward ADS Ptolemy templates
- Easy modification to user-defined configurations

## Linearization Techniques

Following are linearization techniques available in the DesignGuide. To access these tools, select *DesignGuide* > *Linearization DesignGuide* from the ADS Schematic window, and select the appropriate menu commands.

## Feedforward

The following sections provide background details on the use of Feedforward linearization.



Feedforward Linearizer

Increasing demand for spectral efficiency in radio communications makes multilevel linear modulation schemes such as Quadrature Amplitude Modulation more and more attractive. Since their envelopes fluctuate, these schemes are more sensitive to power amplifier nonlinearities, the major contributor of nonlinear distortion in a microwave transmitter. An obvious solution is to operate the power amplifier in the linear region where the average output power is much smaller than the amplifier's saturation power (i.e., Larger output back-off). But this increases both cost and inefficiency as more stages are required in the amplifier to maintain a given level of power transmitted. Thus greater DC power is consumed. Power efficiency is certainly a critical consideration in portable systems where batteries are often used or in small enclosures where heat dissipation is a problem. Another approach to reducing nonlinear distortion is the linearization of the power amplifier.

The power amplifier's characteristics tend to drift with time, due to temperature changes, voltage variations, channel changes, aging, etc. Therefore a robust linearizer should incorporate some form of adaptation.

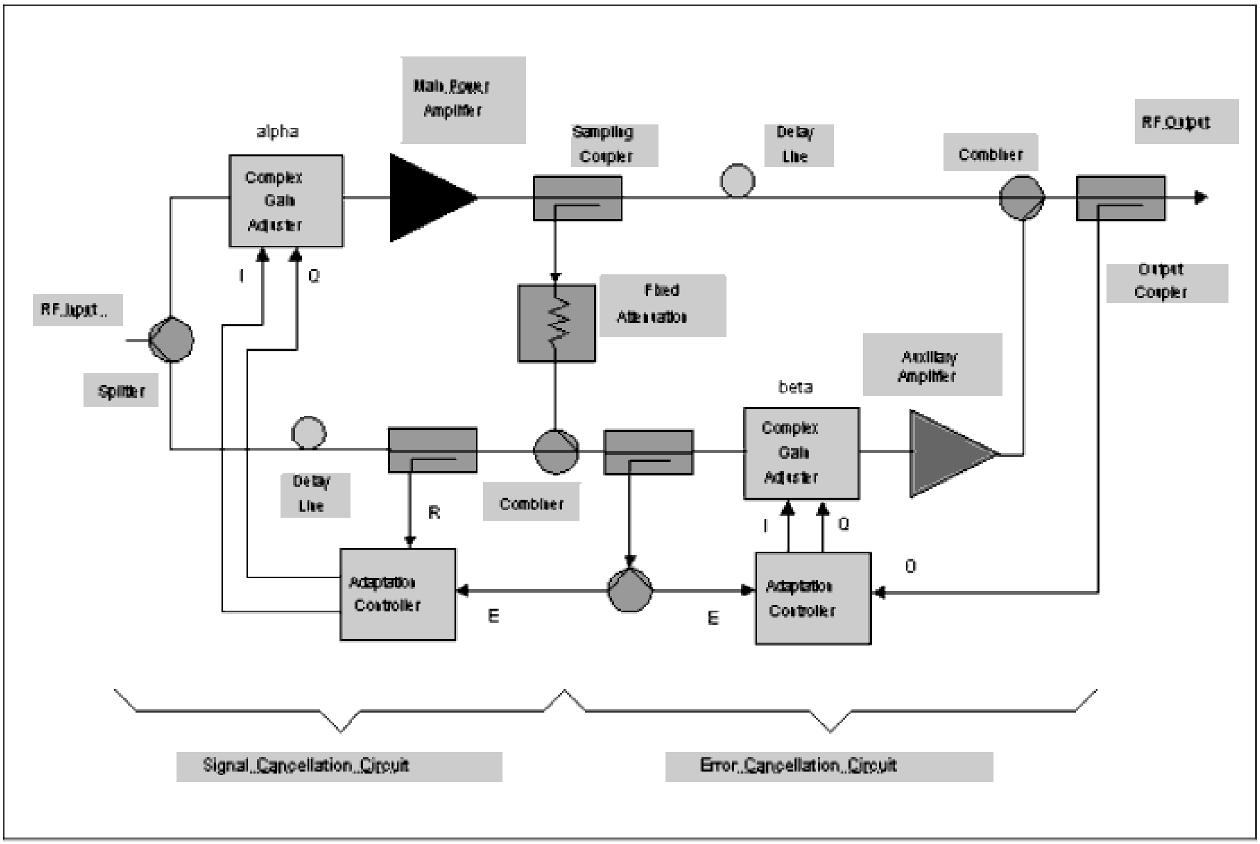
In 1927, H.S. Black of Bell Telephone Laboratories invented the concept of negative feedback as a method of linearizing amplifiers. His idea for feedforward was simple: reduce the amplifier output to the same level as the input and subtract one from the other to leave only the distortion generated by the amplifier. Amplify the distortion with a separate amplifier, then subtract it from the original amplifier output to leave only a linearly amplifier version of the input signal.

## Feedforward Configuration

The feedforward configuration consists of two circuits, the signal cancellation circuit and the error cancellation circuit. The purpose of the signal cancellation circuit is to suppress the reference signal from the main power amplifier output signal, leaving only amplifier distortion, both linear and nonlinear, in the error signal. Linear distortion is due to deviations of the amplifier's frequency response from the flat gain and linear phase. Distortion from memory effects can be compensated by the feedforward technique, since these effects will be included in the error signal. The values of the sampling coupler and fixed attenuation are chosen to match the gain of the main amplifier. The variable attenuation serves the fining tuning function of precisely matching the level of the PA output to the reference.

The variable phase shifter is adjusted to place the PA output in anti-phase with the reference. The delay line in the reference branch, necessary for wide bandwidth operation, compensates for the group delay of the main amplifier by time aligning the PA output and reference signals before combining. The purpose of the error cancellation circuit is to suppress the distortion component of the PA output signal, leaving only the linearly amplifier component in the linearizer output signal. In order to suppress the error signal, the gain of the error amplifier is chosen to match the sum of the values of the sampling coupler, fixed attenuator, and output coupler so that the error signal is increased to approximately the same level as the distortion component of the PA output signal.

## Adaptation Techniques



Adaptive Feedforward Linearization

Several patents concerned with adaptive feedforward systems appeared in the mid-'80's, and many more appeared in the early `90's. These patents dealt with two general methods of adaptation both with and without the use of pilot tones, namely adaptation based on power minimization and adaptation based on gradient signals. The control scheme for the former attempts to adjust the complex vector modulator in the signal cancellation circuit so as to minimize the measured power of the error signal in the frequency band occupied by the reference signal. In the error cancellation circuit, the frequency band is chosen to include only that occupied by the distortion. Once the optimum parameters have been achieved, deliberate perturbations are required to continuously update the coefficients. These perturbations reduce the IMD suppression.

Adaptation using gradient signals is based on continually computing estimates of the gradient of a 3-dimensional power surface. The surface for the signal cancellation circuit is the power in the error signal. This power is minimized when the reference signal is completely suppressed, leaving only distortion. The surface for the error cancellation circuit is the power in the linearizer output signal. The power is minimized when the distortion is completely suppressed from the Power Amplifier output signal.The gradient is continually being computed and therefore no deliberate misadjustment is required.

The ACPR minimization approach uses a frequency translator plus a power detector to select and measure the ACPR. The bandpass filter will capture the adjacent channel power. Care must be taken to ensure that the fundamental signal is rejected. The Digital

Signal Processor performs the adaptation of the work function coefficients based on the scalar value input from the power detector.

The input signals for the complex correlator are the error signal and the reference signal. The error signal is derived by subtracting the input signal from the power amplifier`s output signal. The error signal, if properly aligned, should contain only the resulting distortion generated by the power amplifier. The reference signal is the input to the Feedforward linearizer. The objective of the correlator is to optimize the complex gain adjuster so as to ensure that the two signals are uncorrelated.

## Complex Gain Adjusters

The complex gain adjuster can take on two forms: Polar or Rectangular Implementation. The polar representation requires a voltage-controlled attenuator and phase shifter. The rectangular implementation is of the same form as a quadrature modulator. Either of these configurations need to operate in the linear region where the generated intermodulation products are significantly lower than those generated by the power amplifier. The complex gain adjusters are required to be insensitive to variations across the operational bandwidth.

## RF Predistortion

The linearizer creates a predistorted version of the desired modulation. The predistorter consists of a complex gain adjuster, which controls the amplitude and phase of the input signal. The amount of predistortion is controlled by two nonlinear work functions that interpolate the AM/AM and AM/PM nonlinearities of the power amplifier. Note that the envelope of the input signal is an input to the work functions. The function of the envelope detector is to extract the amplitude modulation of the input RF signal. The delay line in the upper branch compensates for the time delay that occurs as the envelope passes through the work function. Once optimized, the complex gain adjuster provides the inverse nonlinear characteristics to that of the power amplifier. Ideally the intermodulation products will be of equal amplitude but in anti-phase to those created as the two tones pass through the power amplifier. The out-of-band filter will sample the adjacent power interference (ACPI). The function of the DSP is to slowly adapt the work function parameters so that the ACPI is minimized.

## Adaptation Techniques

Several patents concerned with adaptive predistortion systems appeared in the mid-'80's, and many more appeared in the early `90's. These patents dealt with two general methods of adaptation, namely adaptation based on power minimization and adaptation based on gradient signals. The control scheme for the former attempts to adjust the complex gain adjuster in such a way as to minimize the measured power of the error signal in the out-of-band frequency. Once the optimum parameters have been achieved, deliberate perturbations are required to continuously update the coefficients. These perturbations reduce the IMD suppression. Adaptation using gradient signals is based on continually computing estimates of the gradient of a 3-dimensional power surface. The surface for the RF predistorter circuit is the difference between the input signal and the scaled output signal. This power is minimized when the error signal is completely suppressed. The gradient is continually being computed and therefore no deliberate misadjustment is required.

## Work Function

The work function can take on various mathematical forms. The simplest to implement is the polynomial representation, whereby the coefficients are adapted to create the inverse nonlinearity to that of the power amplifier. The work function-based predistorter has limited capability in reducing the level of intermodulation distortion. The envelope modulation is the input parameter for generating the complex gain function.

## FeedForward Combined with RF Predistorter

An RF Predistorter is embedded in the signal cancellation loop of a FeedForward linearizer. The predistorter consists of a complex gain adjuster, which controls the amplitude and phase of the input signal. The predistorter is based on a work function that interpolates the inverse AM/AM and AM/PM nonlinearities of the power amplifier. An envelope detector is used to extract the incoming amplitude modulation, this signal is then used as an input into the work function. The error signal from the signal cancellation loop of the FeedForward linearizer is used to adapt the predistorter coefficients.

The advantages of embedding a RF Predistorter inside a FeedForward Linearizer are that the Intermodulation reduction requirements of the FeedForward Loop alone are reduced. This will reduce the component sensitivities across the band of frequencies. The net result is the overall efficiency improvement of the power amplifier.

There are several techniques for guiding the adaptation of the FeedForward Linearizer. The most commonly used has been the employment of Pilot Tones for optimizing the complex gain adjuster coefficients in both loops. A Pilot Tone can be injected at the input of the FeedForward Linearizer and then monitored at the output of the signal cancellation loop. The first Pilot Tone will ensure that the signal cancellation loop achieves optimum reduction of the fundamental component. The residual signal will contain only the distortion created by the power amplifier. A second Pilot can be injected in the upper branch of the first loop and monitored at the output of the FeedForward linearizer. The second Pilot Tone will be used to ensure that the error cancellation loop achieves optimum reduction of the power amplifier's distortion. Other techniques such as power minimization and signal correlation can also be used in combination with Pilot Tones. These have been discussed in the FeedForward Linearizer section.

Also a number of techniques exist for adapting the RF Predistorter. These have been discussed in the RF predistortion section. The advantage of embedding an RF Predistorter inside the Feedforward Linearizer is that the resultant error signal from the first loop can be used to optimize the RF predistorter work function. Minimization of the adjacent channel power at the error port is an effective technique for optimizing the work function coefficients.

## Analog Predistortion

Predistortion linearization involves constructing a predistorter which has the inverse non-linear characteristics of the power amplifier. Therefore, when the predistorter's output signal is passed through the power amplifier, the distortion components cancel and only the linear components remain. The type of analog predistorter to use is dependent on the nonlinearities generated by the power amplifier. Analog predistorters can be constructed as Square Law or Cubic Law devices or any combination of these two configurations. Typically diodes arranged in various configurations are used to generate the second and third order distorters. For Square Law devices, two diodes are arranged so that the even terms of an equivalent series expansion add together and the odd terms cancel. The opposite is true for the Cubic law devices. An advantage of using diodes is the ability to predistorter over a wide bandwidth. Some of the disadvantages are the power and temperature dependence as well as the inaccuracy in controlling the constructed nonlinearity. Which ultimately leads to a limitation on the amount of IMD reduction achieveable.

An analog predistorter generally has two paths. One carries the fundamental components and the other is the distortion generator. The objectives are the elimination of the fundamental component in the distortion generator path, thereby providing independent control of the distortion relative to the fundamental component. The two paths are time-aligned and then subsequently combined before being presented to the power amplifier.

## LINC

Linear amplification using nonlinear components (LINC) is a technique whereby a linear modulation signal is converted into two constant envelope signals that are independently amplified by power-efficient Class C amplifiers and then combined using a hybrid coupler. The use of power-efficient amplifiers can provide significant improvement in the PAE of the overall system. The envelope conversion operation is a nonlinear process that generates spectral components outside of the modulation bandwidth. Any imbalance between the two Class C amplifiers needs to be eliminated. Otherwise significant ACPI will be generated. A complex gain adjuster can be inserted into one of the branches to adaptively control the balance between the amplifiers. The adaptation process can use either the ACPR minimization approach or the Gradient based correlator approach.

## Cartesian Feedback

Cartesian feedback is based on the classical feedback control system. An error signal is created by subtracting the power amplifier's output from that of the input signal. This error signal is the input to the power amplifier. The limitations of the cartesian feedback linearizer are the achievable bandwidth and system stability. The operational bandwidth is controlled by the amount of delay in the feedback path and the stability is a function of the feedback gain.

## Digital Predistortion

The two most common digital predistortion techniques are the Vector mapping look-up table approach and the Complex gain look-up table approach. The Vector mapping technique stores a compensation Vector into a look-up table for each input signal vector. This approach tends to require a large amount of data storage. The complex gain approach is similar to predistortion whereby the inverse nonlinearity is generated in a look-up table. However, the look-up table provides for a more accurate representation of the inverse nonlinearity. The look-up table is indexed by either magnitude or power. The latter requires less LUT entries and can provide similar intermodulation improvement if the nonlinearity created by the power amplifier is minimal at low levels of input modulation. The resultant error signal generated by subtracting the power amplifier output from the input signal is used to optimize the LUT entries. An adaptive delay is used to properly align the two signals.

The Digital Predistortion linearizer is also supported as a connected solution using Advanced Design System and test equipment. It may be used to linearize amplifier hardware. For more information please view the Guide to Digital Predistortion. A modified version, that also compensates for memory effects, is discussed below.

### Adaptation Using Linear Convergence

Various adaptive algorithms are available that trade speed of convergence with robustness. The simplest of these is linear convergence, whereby the LUT entries are adapted incrementally. The incremental adjustment is proportional to the error vectors magnitude and phase. Some techniques require transformations between polar and rectangular coordinates.

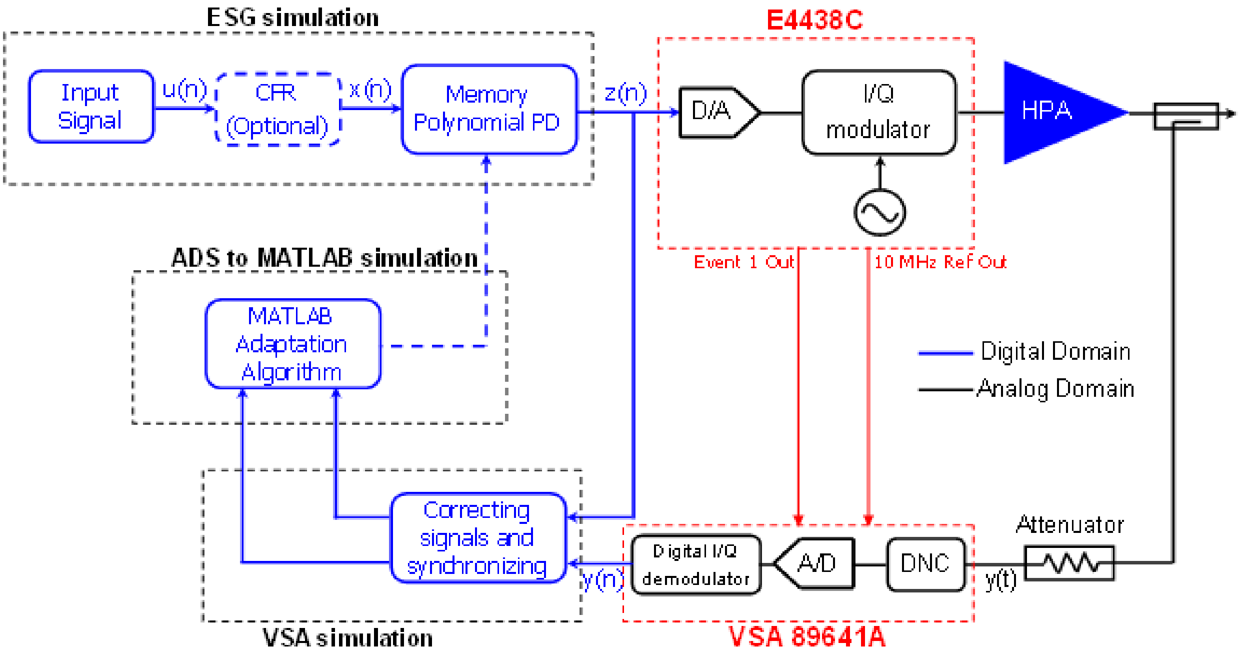
## Memory Effects

Electrical memory effects are caused by varying impedances across the modulation bandwidth. The frequency dependence of the source and load impedances cannot be kept constant for all modulation frequencies. The amplitude and phase of the intermodulation products are dependent on the frequency dependent behavior of the impedances. Careful design of the bias networks can reduce the electrical memory effects. A two-tone simulation can demonstrate the modulation frequency dependence on the 3rd and 5th order IMD products.

Thermal power feedback causes memory effects at low modulation frequencies. Increased power dissipation causes the power amplifier device's junction temperature to increase which in turn alters the amplifier's gain. These memory effects are observed as the envelope varies over time. Modeling these long time constant effects requires a form of thermal power feedback.

## Digital Predistortion with Memory Effects (technique using ADS/ESG/VSA/Matlab)

This techniques uses a combination of hardware and simulation to perform Digital Predistortion with Memory Effects. This requires working knowledge of the ESG for capturing the signal waveform, the VSA 89600 for generating the signal waveform, the VSA 89600 software, and Matlab for co-simulation with ADS.



> The block diagram of the digital predistortion with memory effects and CFR

The overview of this technique is described below.

## Analog/RF Examples

The following sections provide details on the Analog/RF examples.To access these examples, select *DesignGuide* > *Linearization DesignGuide* from the ADS Schematic window, and select the appropriate example.

### Feedforward

Step 7 in the Feedforward menu is an example of a feedforward linearizer. The first loop consists of a power amplifier and a complex gain adjuster, which is adjusted using a complex correlator. The power amplifier is a transistor level design, which is easily replaced by the user-defined component. The input power level as well as the input frequency needs to be set. The power amplifier group delay needs to be compensated on the lower branch of the first loop. The second loop consists of an auxiliary amplifier along with a complex gain adjuster, which is optimized using the ACPR minimization technique. If a transistor level auxiliary amplifier is being used, the upper branch of the second loop also needs to have a compensating group delay.

The feedforward design consists of an 8-step process to develop a double loop structure. The design process begins with an optimization of the first loop and subsequent designs build on this structure. Once the complete feedforward structure has been developed, the two-tone input can be replaced by the user-defined input modulation. Examples are included for an IS-95 CDMA signal, 16 QAM signal as well as a pi/4 DQPSK signal.

The simulation results from the 8th step of the feedforward linearizer demonstrate the optimization that can be achieved using a two-tone input. The optimization algorithm can be changed to reflect the adaptation process to be used in the user defined system.

## RF Predistorter

Step 5 in the RF Predistorter menu is a 5th-order polynomial work function based RF predistorter. The adaptation technique is based on the gradient approach using a complex correlator. The output signal from the power amplifier is subtracted from the input reference signal. If properly aligned, the resultant error signal will consist of only the distortion generated by the power amplifier. The work function coefficients can then be optimized so as to minimize the error signal. The input to the work function is the squared envelope of the incoming signal. A group delay is required to compensate for the delay from the envelope detector, and a delay is required in the feedback path to compensate for the delay from the upper branch.

The RF Predistorter design consists of a 7-step process to develop a gradient-based optimized structure. The design process begins with an optimization using the ACPR minimization technique and subsequent designs build on this structure. Once the complete RF Predistorter structure has been developed, the two-tone input can be replaced by the user-defined input modulation. Examples are included for a 16 QAM signal, IS-95 CDMA signal, as well as a pi/4 DQPSK signal.

## FeedForward combined with RF Predistorter

Step 10 in the Feedforward with RF Predistorter menu is an example of a feedforward linearizer with an embedded RF predistorter. The first loop consists of a power amplifier and a complex gain adjuster, which is adjusted using a complex correlator. The power amplifier is a transistor level design, which is easily replaced by the user-defined component. The input power level as well as the input frequency need to be set.

The power amplifier group delay needs to be compensated on the lower branch of the first loop. Also incorporated in this loop is a work function based RF Predistorter . The optimization of the RF Predistorter is easiest achieved by minimizing the ACPR at the error port. The second loop consists of an auxiliary amplifier along with a complex gain adjuster, which is optimized using the Pilot Tone approach. If a transistor level auxiliary amplifier is being used, the upper branch of the second loop also needs to have a compensating group delay.

The feedforward combined with RF Predistorter design consists of a 10-step process to develop a double-loop structure. The design process begins with an optimization of the first loop and subsequent designs build on this structure. Once the complete structure has been developed, the two-tone input can be replaced by the user-defined input modulation.
The optimization algorithm can be changed to reflect the adaptation process to be used in the user-defined system.

## Analog Predistortion

The Analog Predistorter consists of a 3-Step Cubic Law process and a 3-Step Square law process. Both predistorters are based on using diodes in various configurations to generate the distortion. The diodes can be biased to better approximate the type of nonlinear behavior that is required. The predistorters consist of two paths; one to generate the nonlinearity and the other to pass the fundamental components. A hybrid is used in the distortion generation path for eliminating the fundamental component. A complex gain adjuster is then used to control the amplitude and phase of the distortion relative to the fundamental component.

The square law device optimizes the bias voltage to reduce any third order nonlinearity. The impedance in the 4th port of the hybrid is adjusted in order to eliminate the fundamental component at the output of the hybrid. Step 3 of the analog cubic law predistorter is an example of the predistortion of a power amplifier.

The cubic law device is not biased in this configuration. It consists of two anti-parallel diodes to create the cubic behavior. A hybrid is also used in this distorter to eliminate the fundamental component.Step 3 of the analog square law predistorter is an example of the predistortion of a power amplifier.

## LINC

Linear amplification using nonlinear components (LINC) consists of Class C power amplifiers along with a nonlinear operation that converts the fluctuating envelope into a constant amplitude envelope. The conversion process is nonlinear and subsequently generates a significant amount of spectral spreading. The hybrid combiner at the output eliminates the out-of-band components. However, any misalignment between the two Class C amplifiers will result in some residual out-of-band components.

The LINC design consists of a 5-step process to develop an ACPR minimization-based optimized structure. The design process begins with an optimization with a two-tone input and subsequent designs build on this structure. Once the complete LINC structure has been developed, the two-tone input can be replaced by the user-defined input modulation. An example is included for a 16 QAM, IS95 CDMA and a pi/4 DQPSK signal.

The simulation results for LINC using a pi/4 DQPSK modulation demonstrate the ACPR performance of the power amplifier. The results show how the nonlinear transformation converts the linear modulation into two constant envelope modulations. The resultant frequency spreading into the adjacent channel is also observed. Upon combining, the output signal is reconstructed and has recovered the proper levels of adjacent channel interference.

## Cartesian Feedback

The cartesian feedback linearizer consists of a power amplifier along with a quadrature modulator and demodulator. The feedback error signal is created by subtracting the baseband input signal from the power amplifier's demodulated output signal. The transistor level power amplifier can be replaced by a user-defined component.

The demodulated I and Q signals at the output of the power amplifier are fed back to the summing input of the comparator/filter circuit, after a 180-degree phase shift. The comparator/filter circuit will predistort its output to maintain a virtual ground at the comparator summing node. This will occur when both inputs to the comparator/filter circuit are in phase for an open loop. When the loop is closed, the input to the comparator/filter circuit will be equal but in opposite phase.

To get loop stability, the comparator/filter circuit uses a lowpass filter to limit the loop bandwidth. The cutoff frequency must be sufficiently wider than the bandwidth spread due to the amplifier nonlinearity. Linearity is limited by two factors, the loop gain and the accuracy of the feedback path. The loop gain has to be as large as possible, but is limited by the loop stability, which in turn is closely dependent on the phase response. Adjustment of the phase shifter is critical. With the loop opened, the phase should be adjusted so that there is no phase rotation of the demodulated I and Q signals with respect to the I and Q signals at the input of the comparator/filter circuit.

The optimization process for the cartesian feedback system is demonstrated. The relative improvement in the level of ACPR can be measured by comparing the open and closed loop responses. An example is included for a 16 QAM, IS95 CDMA and a pi/4 DQPSK signal.

## Digital Predistortion

The digital predistorter consists of a complex gain adjuster along with a polynomial-based work function. The standard look-up table has been replaced by a work function for demonstration purposes. One of the key features that is included using this structure is the quantization noise introduced by the A to D. The number of bits of the A/D will determine the size of the Look-Up Table. The polynomial structure can be used to fit the LUT entries in a DSP implementation.

The output of the power amplifier is subtracted from the input reference, resulting in an error signal that should contain only distortion, if properly aligned. The resultant error signal would be used to update the LUT entries or equivalently the polynomial coefficients. An example is included for a 16 QAM, IS95, CDMA2000 and a pi/4 DQPSK signal.

The Digital Predistortion linearizer is available as a connected solution using ADS and test equipment. It is documented in the Guide to Digital Predistortion. A modified version that compensates for memory effects is documented below.

### Memory Effects

The electrical memory effects of a power amplifier are observed in the Short Time Constant example. A two tone test is performed in which the frequency spacing is altered. The modulation frequency dependence on the 3rd and 5th order intermodulation products can be observed. Any asymmetry in the lower and upper sideband IMD products will limit the amount of predistortion improvement that is achieveable.

The thermal memory effects can be observed for various input modulations. The ACPR is plotted as a function of the memory delay. Examples are included for IS-95, CDMA2000 and pi/4 DQPSK. A thermal memory effect compensator is demonstrated for various input modulations.

## ADS Ptolemy Examples

The following sections provide details on the ADS Ptolemy examples. To access these examples, select *DesignGuide* > *Linearization DesignGuide*> *ADS Ptolemy (Demos/Templates)* from the ADS Schematic window, and select the appropriate example.

### Feedforward

The single adaptive loop ADS Ptolemy example includes a multi-tone input. This example demonstrates a fast rate of convergence because of the gradient based optimization technique.

A number of feedforward configurations are developed in ADS Ptolemy. The 1st and 2nd loops can be optimized using either complex correlators or the ACPR minimization technique. Some of the demos store the data while others open windows to observe the adaptation process. A couple of templates use transistor level power amplifiers you can replace these with your own power amplifiers.

The single loop feedforward linearizer performance is demonstrated in this example. The adaptation process is very fast because of the use of the gradient technique. The gradient technique is based on using a complex correlator. The initial intermodulation products are at -25 dBc, then are quickly reduced to a final state level of approximately -80 dBc.

This example is a real-time demonstration of the convergence of a RF Predistorter based on the ACPR minimization technique. The work function is a 5th-order polynomial that is fed by the envelope of the input signal. The adaptation algorithm is based on the secant method, whereby an approximation for the derivatives of the ACPR with respect to the work function coefficients is calculated. The work function consists of a 5th-order polynomial which is a function of the input signal envelope.

## Digital Predistorter

This example is a real-time demonstration of the convergence of a digital predistorter based on the linear convergence technique. The envelope of the input signal indexes the RAM look-up tables. The look-up table entries are fed to the complex gain adjuster. In this particular configuration, the data registers and RAM tables need proper triggering to ensure that the data is valid before being written or read. The error signal is derived by subtracting the input reference signal from the power amplifier's output. This error signal is used to update the look-up tables using a linear convergence technique.

## RF Predistortion

The linearizer creates a predistorted version of the modulated signal. The predistorter consists of a complex gain adjuster which controls the amplitude and phase of the input signal. The amount of predistortion is controlled by two nonlinear work functions that interpolate the AM/AM and AM/PM nonlinearities of the power amplifier. The feedback path samples a portion of the undesired spectrum (ACPR) which is minimized by optimizing the polynomial work function coefficients. The four coefficients of the polynomial control the cubic and quintic nonlinearities. These coefficients are slowly optimized using a discrete implementation of a least mean squared direct search technique.

## Digital Predistortion With Memory Effects

In digital predistortion for memory effects compensation, the most well known structure is based on the polynomial method, so called, memory polynomial predistortion using indirect learning algorithm. Memory polynomial predistortion is designed in Advanced Design System using finite impulse response (FIR) filters for each order of polynomial. Coefficients of the filters are generated from MATLAB by running ADS-to-MATLAB simulation. Please refer to the block diagram of the system. This technique uses a combination of ADS, a VSA , an ESG and Matlab. The set up file is generated from the VSA 89600 software and is subject to the operating system requirements for this software. Please refer to the VSA user documentation on how to save the set up file. The setup file needs to be placed in the data folder of the ADS project

1. *DigitalPredistortionMem_ESGSink.dsn*

   > DesignGuide/Linearizer/Digital Predistortion (Ptolemy/ESG-VSA)/Memory Compensation Predistorter using ESG-VSA-Matlab / Run ESG Simulation (Initialization)

   Open this design and make sure that Initialization "Yes" in the Var Eqn at the bottom, and run simulation after also checking the other settings, such as ESGCarrierFrequency, ESGAmplitude_dBm, Order, and so on (in this schematic, polynomial order of predistortion is only designed for fifth or seventh order including even terms, so users can only choose between them). The DUT should be connected and powered when running this simulation.
2. *DigitalPredistortionMem_VSASource.dsn*

   > DesignGuide/Linearizer/Digital Predistortion (Ptolemy/ESG-VSA)/Memory Compensation Predistorter using ESG-VSA-Matlab / Run VSA Simulation

   Open this design and run simulation after also checking other settings. At this point, you can run the simulation again after changing the VSANormalizationFactor in the Var Eqn according to the Normalization Factor result in the page of memory effects of the data display or you can proceed to Step 3 (Step 3 will perform normalization from MATLAB). Step 2 automatically opens the VSA software window depending on the setting.
3. *ADSToMatab.dsn*

   > DesignGuide/Linearizer/Digital Predistortion (Ptolemy/ESG-VSA)/Memory Compensation Predistorter using ESG-VSA-Matlab/Run ESG Simulation/Generate Memory Polynomial Coefficients

   Open this design and run the simulation. This simulation generates coefficients for filters in memory polynomial predistortion and saves them as .txt file that can be read in ESG simulation. The MATLAB code, TdlPd(Input#1, Input#2, Order, Memory), implements scaling and the least square algorithm (scaling is also performed in MATLAB for the case that the VSANormalizationFactor in Step 2 isn't properly set up. Order should be the same as the Order from Step 1).

4. *DigitalPredistortionMem_ESGSink.dsn*

    > DesignGuide/Linearizer/Digital Predistortion (Ptolemy/ESG-VSA)/Memory Compensation Predistorter using ESG-VSA-Matlab/ Run ESG Simulation (with Predistortion)

    Open this design and make sure that Initialization is changed to "No" for the memory polynomial predistortion, run simulation, and take a close look at the predistorted signal from the data display window. In addition, the maximum input magnitude coming to the memory polynomial predistortion block is required to be normalized to 1 (This is required for CFR or different applications, which don't have a peak magnitude close to 1). - There might be an error message if you don't close the VSA software window.
    Note1

    Step 4 ends one iteration. For most of power amplifiers, one iteration is good enough for achieving good performance due to least square solution.

    Note2

    Step 2 to Step 4, repeat if required.

## Crest Factor Reduction

Crest Factor Reduction (Peak-to-average power ratio reduction) block for WCDMA multi-carrier applications can be inserted in DigitalPredistortionMem_ESGSink.dsn in order to enhance the efficiency of the power amplifier. Algorithm was implemented based on Reference CFR Ref 1 and CFR Ref 2. The CFR block consists of a baseband clipper, a noise shaper for WCDMA multi-carrier applications. In order to test the CFR, open Test_CFR_Signal.dsn by using the schematic menu DesignGuide/Linearizer/Digital Predistortion (Ptolemy/ESG-VSA)/Crest Factor Reduction/ CFR Algorithm Simulation. There is a scaling factor that needs to be set up in order to enhance the performance of the CFR. It is calculated by an equation as shown in Data Display Window (Test_CFR_Signal.dds) after simulation. To further enhance the performance of the CFR, multiple stages of the CFR block can be applied according to Reference CFR Ref 2. Threshold (<100) is a percentage ratio relative to the input maximum magnitude, which is required to be properly set up.

Note

Coefficients for the filter in the noise shaper were generated in MATLAB based on 38.4 MHz of sampling rate and WCDMA single-carrier, so if the sampling rate or the input signal bandwidth is changed, the filter coefficients should be changed. It can be done in MATLAB using built-in functions such as, fir1, firls, firpm, and so on.

# Reference

The following sections provide useful reference information for the Linearization DesignGuide.

## Template Reference Guide

Following are the available templates in the Linearization DesignGuide.

### Feedforward Linearization

*FF_step1* (Signal Cancellation Loop Contours)
*FF_step2* (Optimization of Coefficients in Signal Cancellation Loop)
*FF_step3* (Optimization of Coefficients using Complex Correlator)
*FF_step4* (Adjustment of Error Cancellation Loop Gain)
*FF_step5* (Optimization of Coefficients for Error Cancellation Loop)
*FF_step6* (Optimization of 2nd Loop Coefficients using 3rd-order IMD Minimization)
*FF_step7* (Optimization of 2nd Loop Coefficients using ACPR Minimization)
*FF_step8* (Optimization of Coefficients using ACPR Minimization)
*FF_16QAM* (ACPR Performance with 16 QAM Signal)
*FF_16QAMop* t (ACPR Optimization with 16 QAM Signal)
*FF_CDMA2000Rev* (ACPR Performance with CDMA2000 Signal)
*FF_IS95Rev* (ACPR Performance with IS95 CDMA Signal)
*FF_IS95Revopt* (ACPR Optimization with IS95 CDMA Signal)
*FF_Pi4DQPSK* (ACPR Performance with Pi/4 DQPSK Signal)
*FF_Pi4DQPSKopt* (ACPR Optimization with Pi/4 DQPSK Signal)

### RF Predistorter

*RFPred_step1* (Contour Plot of 3rd-order Coefficients)
*RFPred_step2* (Optimization of Coefficients based on IMD Reduction)
*RFPred_step* (3rd-order Coefficient Sensitivity about Optimum)
*RFPred_step4* (5th-order Coefficient Sensitivity about Optimum)
*RFPred_step5* (Signal Cancellation Loop Optimization)
*RFPred_step6* (IMD Optimization using Signal Cancellation Loop)
*RFPred_step7* (Error Minimization using Signal Cancellation Loop)
*RFPred_16QAM* (ACPR Performance with 16 QAM Signal)
*RFPred_IS95Rev* (ACPR Performance with IS-95 CDMA Signal)
*RFPred_Pi4DQPSK* (ACPR Performance with pi/4 DQPSK Signal)

### FeedForward combined with RF Predistorter

*FF_with_RFPred_step1* (Linear Coefficients Optimization using Complex Correlator)
*FF_with_RFPred_step2* (Nonlinear Coefficients Optimization using Power Minimization)
*FF_with_RFPred_step2a* (Linear and Nonlinear Coefficients Optimization at Error

Port)
*FF_with_RFPred_step3* (Pilot Tone Optimization in Signal Cancellation loop)
*FF_with_RFPred_step4* (Pilot Tone and IMD Power Minimization at Error Port)
*FF_with_RFPred_step5* (Pilot Tone Optimization in Error Cancellation loop)
*FF_with_RFPred_step6* (Two Pilot Tones used for Optimization of Linear Coefficients)
*FF_with_RFPred_step7* (Two Pilot Tones Optimization and IMD Power Minimization)
*FF_with_RFPred_step8* (Output Pilot Tone Removal using Re-injected Pilot at Error Port)
*FF_with_RFPred_step9* (Coefficients Optimization using 2 Pilot Tones and Re-injected Pilot)
*FF_with_RFPred_step10* (Pilot Tones and Re-injected Pilot Tone and IMD Power Optimization)

## Analog Predistortion

*Analog_CubicPred_step1* (Optimization of Cubic predistorter)
*Analog_CubicPred_step2* (Power and Frequency Dependence of Cubic Law Predistorter)
*Analog_CubicPred_step3* (Cubic Law Predistortion of Power Amplifier)
*Analog_SquarePred_step1* (Square Law Predistorter Dependence on Power and Bias Voltage)
*Analog_SquarePred_step2* (Optimization of Square Law Predistorter)
*Analog_SquarePred_step3* (Square Law Predistortion of Power Amplifier)

## LINC

*LINC_step1* (Demonstration of Spectral Characteristics)
*LINC_step2* (Demonstration of Performance Sensitivity)
*LINC_step3* (Swept Complex Gain Adjuster Coefficients)
*LINC_step4* (Optimized Complex Gain Adjuster Coefficients)
*LINC_step5* (ACPR Minimization with Complex Gain Adjuster)
*LINC_16QAM* (ACPR Performance with 16 QAM Signal)
*LINC_IS95Rev* (ACPR Performance with IS95 Rev. Link Signal)
*LINC_Pi4DQPSK* (ACPR Performance with pi/4 DQPSK Signal)

## Cartesian Feedback

*CartesianFBoff_16QAM* (ACPR Performance Open Loop)
*CartesianFBon_16QAM* (ACPR Performance Closed Loop)
*CartesianFBoff_Pi4DQPSK* (ACPR Performance Open Loop)
*CartesianFBon_Pi4DQPSK* (ACPR Performance Closed Loop)
*CartesianFBoff_IS95Rev* (ACPR Performance Open Loop)
*CartesianFBon_IS95Rev* (ACPR Performance Closed Loop)

## Digital Predistortion

*DigPred_step1* (AM/AM and AM/PM Compensation Function)
*DigPred_step2* (Finite Look-Up Table Size)
*DigPred_step3* (Complex Correlator Optimization of Linear Coefficients)
*DigPred_step4* (Optimization of Predistorter Based on Error Minimization)
*DigPred_step5* (Optimization of Linear Coefficients using a Pilot Tone)
*DigPred_step6* (Optimization of Linear and Nonlinear Coefficients)
*DigPred_16QAM* (ACPR Performance)
*DigPred_Pi4DQPSK* (ACPR Performance)
*DigPred_IS95Rev* (ACPR Performance)
*DigPred_CDMA2000* (ACPR Performance)

### Memory Effects

*Memory_Effects_STC* (Electrical Memory Effects, 2 Tone Simulation)
*Memory_Effects_LTC_CDMA2000* (Thermal Memory Effects, CDMA2000 Input)
*Memory_Effects_LTC_IS95* (Thermal Memory Effects, IS-95 CDMA Input)
*Memory_Effects_LTC_Pi4DQPSK* (Thermal Memory Effects, Pi/4 DQPSK Input)
*Memory_Comp_LTC_CDMA2000* (Thermal Memory Compensation, CDMA2000 Input)
*Memory_Comp_LTC_IS95* (Thermal Memory Compensation, IS-95 Input)
*Memory_Comp_LTC_Pi4DQPSK* (Thermal Memory Compensation, Pi/4 DQPSK Input)

*DigitalPredistortionMem_ESGSink* (memory effects compensation ADS/ESG/VSA/Matlab)
*DigitalPredistortionMem_VSASource* (source setup for memory effects compensation ADS/ESG/VSA/Matlab)
*ADSToMatlab* (generate coefficients for filter in memory predistortion)

### Crest Factor Reduction

*CFR* (Peak-to-average power ratio reduction for WCDMA multi-carrier)

### ADS Ptolemy

*FFD_PM_2T_SL* (Two-Tone Input, Single Loop, ACPR Minimization)
*FFD_GD_MT_SL* (Multi-Tone Input, Single Loop, Gradient Optimization)
*FFD_PM_2T_SL* (Multi-Tone Input, Single Loop, ACPR Minimization)
*FFD_PM_95_SL* (IS-95 CDMA Input, Single Loop, ACPR Minimization)
*Demo_FeedForward* (Two-Tone Input, Double Loop, Gradient Optimization)
*FFT_PM_2T_SL* (Two-Tone Input, Single Loop, ACPR Minimization)
*FFT_PM_95_SL* (IS-95 CDMA Input, Single Loop, ACPR Minimization)
*WorkFunct_real_PA_Demo* (RF Predistortion Demo)
*DPLUT_idealPA* (Digital Predistortion Demo)

## Parameter Definitions

**[RFfreq]** RF frequency (MHz): The center frequency of the operational bandwidth.

**[Delta]** the frequency spacing of a two tone signal (MHz): One half the frequency separation for a two-tone input signal.

[**Alpha_I]** Complex gain adjuster In-phase control: The in-phase control parameter of the complex gain adjuster in the first loop.

**[Alpha_Q]** Complex gain adjuster Quadrature-phase control: The quadrature-phase control parameter of the complex gain adjuster in the first loop.

**[Group_Delay]** Group Delay (ns): The power amplifier group delay compensation.

**[V_GB]** quadrature output of complex correlator: The complex correlator output from the quadrature branch.

**[V_GA]** in-phase output of complex correlator: The complex correlator output from the in-phase branch.

**[Beta_I]** Complex gain adjuster In-phase control: The in-phase control parameter of the complex gain adjuster in the second loop.

**[Beta_Q]** Complex gain adjuster Quadrature-phase control: The quadrature-phase control parameter of the complex gain adjuster in the second loop.

**[LOfreq]** LO frequency (MHz): The frequency translation of the ACPR minimization converter.

**[Pout_dBcIMD]** Carrier to 3rd-order IMD: The output carrier to 3rd-order intermodulation power at the output.

**[Pout_dBcIMDL]** Lower Carrier to 3rd-order IMD: The lower output carrier to 3rd-order intermodulation power at the output.

**[Pout_dBcIMDU]** Upper Carrier to 3rd-order IMD: The upper output carrier to 3rd-order intermodulation power at the output.

**[P_IFoutL]** IF output power of lower 3rd-order IMD: The lower sideband power of the 3rd-order intermodulation product from the ACPR minimization converter.

**[P_IFoutU]** IF output power of upper 3rd-order IMD: The upper sideband power of the 3rd-order intermodulation product from the ACPR minimization converter.

**[tstep]** step time: The envelope simulation time step.

**[tstop]** stop time: The envelope simulation stop time.

**[numSymbols]** number of symbols: The number of symbols in the envelope simulation.

**[sam_per_bit]** samples per bit: The number of samples that represent each bit.

**[bit_rate]** bit rate: The bit rate for the envelope simulation.

**[PAE]** power added efficiency: The power-added efficiency of the power amplifier.

**[Pavs_Watts]** average input power (watts): The average input power to the linearizer in watts.

**[Pdc]** DC input power: The average DC power consumption of the power amplifier.

**[ChannelPower_dBm]** output channel power (dBm): The output power from the linearizer in dBm.

**[TransACPR]** adjacent channel power ratio at linearizer output: The power ratio between the main channel and the adjacent channels.

**[TransACPR_PA]** adjacent channel power ratio at power amplifier output: The power ratio between the main channel and the adjacent channels.

**[mainlimits]** frequency limits of the main channel: The frequency limits of the main channel.
**[UpChlimits]** frequency limits of the upper channel: The frequency limits of the upper channel.
**[LoChlimits]** frequency limits of the lower channel: The frequency limits of the lower channel.
**[numpts]** number of points: The number of symbols used in the envelope simulation.
**[sam_per_sym]** samples per symbol: The number of samples per symbol used in the envelope simulation.
**[Z_s]** input power source impedance: The impedance of the input power source.
**[filt_delay_syms]** number of symbol delays in shaping filter: The number of symbols of delay in the input shaping filter.
**[sym_rate]** symbol rate: The symbol rate in the envelope simulation.
**[Alpha_3rd]** 3rd-order work function real coefficient: The 3rd-order real coefficient for the polynomial work function.
**[Alpha_5th]** 5th-order work function real coefficient: The 5th-order real coefficient for the polynomial work function.
**[Alpha_7th]** 7th-order work function real coefficient: The 7th-order real coefficient for the polynomial work function.
**[Beta_3rd]** 3rd-order work function imaginary coefficient: The 3rd-order imaginary coefficient for the polynomial work function.
**[Beta_5th]** 5th-order work function imaginary coefficient: The 5th-order imaginary coefficient for the polynomial work function.
**[Beta_7th]** 7th-order work function imaginary coefficient: The 7th-order imaginary coefficient for the polynomial work function.
**[P_IMD]** intermodulation power: The amount of intermodulation power.
**[P_IMD3rd_L]** 3rd-order intermodulation power of lower sideband: The level of the 3rd-order intermodulation power of the lower sideband.
**[P_IMD3rd_U]** 3rd-order intermodulation power of upper sideband: The level of the 3rd-order intermodulation power of the upper sideband.
**[P_IMD5th_L]** 5th-order intermodulation power of lower sideband: The level of the 5th-order intermodulation power of the lower sideband.
**[P_IMD5th_U]** 5th-order intermodulation power of upper sideband: The level of the 5th-order intermodulation power of the upper sideband.
**[P_IMD7th_L]** 7th-order intermodulation power of lower sideband: The level of the 7th-order intermodulation power of the lower sideband.
**[P_IMD7th_U]** 7th-order intermodulation power of upper sideband: The level of the 7th-order intermodulation power of the upper sideband.
**[Group_Delay_PA]** power amplifier group delay: The group delay of the power amplifier.
**[spacing]** two tone frequency spacing: The frequency separation value between the two tones at the input to the linearizer.
**[rmax]** maximum voltage at the input: The maximum voltage excursion at the input of the linearizer.

**[Delta_Gain]** differential gain: The gain imbalance between amplifiers.

**[Delta_Phase]** differential phase: The phase imbalance between amplifiers.

**[Pavs_in]** average source input power: The source average input power.

**[our_ctm]** carrier to 3rd-order IMD: The carrier to 3rd-order intermodulation level.

**[V_IFoutL]** IF output voltage of lower 3rd-order IMD: The lower sideband voltage of the 3rd-order intermodulation product from the ACPR minimization converter.

**[V_IFoutU]** IF output voltage of upper 3rd-order IMD: The upper sideband voltage of the 3rd-order intermodulation product from the ACPR minimization converter.

**[RFpwr]** __ RF input power: The RF input power.

**[Filter_delay_syms]** pulse shaping filter symbol delay: The number of symbol delays in the pulse shaping filter.

**[Vdd]** drain voltage: The power amplifier drain supply voltage.

**[vbaseband]** baseband input voltage: The baseband modulation voltage.

**[fbaseband]** baseband modulation frequency: Te baseband modulation frequency.

**[extrapts]** extra points in simulation: The number of additional symbols in the envelope simulation.

**[Start_Freq]** start frequency for sweep: The start frequency for the simulation.

**[Stop_Freq]** stop frequency for sweep: The stop frequency for the simulation.

**[Step_Freq]** step frequency for sweep: The step frequency for the simulation.

**[our_pgain]** power gain of amplifier: The power amplifier power gain profile.

**[our_dlp]** linear phase deviation: The deviation from a linear phase.

**[Pavs_dBm]** source input power: The average source input power.

**[our_pae]** power added efficiency: The power-added efficiency of the power amplifier.

**[our_dcrf]** DC to RF power efficiency: The DC-to-RF power efficiency of the power amplifier.

**[Gain]** power gain: The gain of the power amplifier.

**[Time_Step]** time step: The step time of the envelope simulation.

**[Freq_Center]** center frequency: The center frequency of the input signal.

**[S_per_Symbol]** samples per symbol: The number of samples per symbol in the simulation.

**[Averager]** averager in the adaptation algorithm: The number of observations taken before a decision is made.

**[Alpha_Rate]** adaptation rate: The adaptation rate of the algorithm in the 1st loop.

**[Beta_Rate]** adaptation rate: The adaptation rate of the algorithm in the 2nd loop.

**[DataRate]** baseband data rate: The baseband modulation rate.

**[ChipRate]** chip data rate: The chip rate of the spread spectrum PN sequence.

**[SamplerperChip]** samples per chip: The number of samples per chip.

**[FIRtaps]** Finite Impulse Response taps: The number of taps in the FIR filter.

**[Freq_IMD]** 3rd-order IMD frequency: The 3rd-order intermodulation frequency.

**[Fund_Lower]** fundamental frequency of lower sideband: The fundamental frequency of the lower sideband.

**[Fund_Upper]** fundamental frequency of upper sideband: The fundamental

frequency of the upper sideband.
**[Number_Taps]** hilbert transform taps: The number of taps in the hilbert transform.
**[training]** training period: The number of observations required for training.

## Encoded Subcircuits

The following section provides useful reference information for the encoded subcircuits in the Linearization DesignGuide.

Complex_Gain_Adjuster_linlib
Used in the Ptolemy simulations, which operate in Floating Point Domain. This component is an ideal vector modulator implementation. The input signal is split into two branches, each branch being individually controlled by inputs I and Q. The output is the sum of the two branches. The two branches of the vector modulator are in phase quadrature and the mixer elements are implemented using ideal multipliers. The vector modulator can achieve phase shifts anywhere in the range [0,360] as well as amplitudes [0, infinity].

Complex_Gain_Adjuster_RealTime_linlib
Used in the Ptolemy simulations, which operate in Timed Domain. This component is an ideal vector modulator implementation. The input signal is split into two branches, each branch being individually controlled by inputs I and Q. The output is the sum of the two branches. The two branches of the vector modulator are in phase quadrature and the mixer elements are implemented using ideal multipliers. The vector modulator can achieve phase shifts anywhere in the range [0,360] as well as amplitudes [0, infinity].

ComplexGainAdjuster_linlib
Used in the Analog/RF simulations. This component is an ideal vector modulator implementation. The input signal is split into two branches, each branch being individually controlled by inputs I and Q. The output is the sum of the two branches. The two branches of the vector modulator are in phase quadrature and the mixer elements are implemented using ideal multipliers. The vector modulator can achieve phase shifts anywhere in the range [0,360] as well as amplitudes [0, infinity].

HB1ToneFswpSub_linlib
Used in the Analog/RF simulations. This element is a nonfunctional component.

HB1TonePswpSub_linlib
Used in the Analog/RF simulations. This element is a nonfunctional component.

Source_IS95_Revlink_linlib
Used in the Analog/RF simulations. This element is a IS-95 source generated from the Library. The dataset used contains baseband I and Q versus time data, which uses a FIR filter that is longer than the IS-95 specification. The bit rate is 1.2288 MHz, sampled at 4 bits per symbol.

Source_Pi4DQPSK_linlib
Used in the Analog/RF simulations. This element is a Pi/4 DQPSK source that uses a root raised cosine filter to generate the I and Q signals. The data rate is 24.3 KHz, sampled at 10 samples per symbol.

Source_QAM_16_linlib
Used in the Analog/RF simulations. This element is a 16 QAM source that h uses root raised cosine filter to generate the I and Q signals. The data rate is 24.3 KHz, sampled at 10 samples per symbol.

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