

# **Practical Digital Pre-Distortion Techniques for PA Linearization in 3GPP LTE**

Jinbiao Xu Agilent Technologies Master System Engineer



**Agilent Technologies** 

SystemVue DPD Jinbiao XU May 26, 2010

# Agenda

- Digital PreDistortion----Principle
- Crest Factor Reduction
- Digital PreDistortion Simulation
- Digital PreDistortion Hardware Verification



### **Digital Pre-Distortion----- Principle**



## **Digital Pre-Distortion----- Principle**

The DPD-PA cascade attempts to combine two nonlinear systems into one linear result which allows the PA to operate closer to saturation. The objective of digital predistorter is to have  $y(t) \approx Cx(t)$ , where C is a constant.



The most important step is to extract PA nonlinear behavior accurately and efficiently.





## **Memory Polynomial Algorithm**

- As the signal (such as 3GPP LTE) bandwidth gets wider, power amplifiers begin to exhibit memory effects. Memoryless (LUT) pre-distortion can achieve only very limited linearization performance.
- Volterra series is a general nonlinear model with memory. It is unattractive for practical applications because of its large number of coefficients.
- Memory polynomial reduces Volterra's model complexity. It is interpreted as a special case of a generalized Hammerstein model. Its equation is as follows:

$$z(n) = \sum_{k=1}^{K} \sum_{q=0}^{Q} a_{kq} y(n-q) |y(n-q)|^{k-1}$$

K is Nonlinearity order and Q is Memory order

**Memory Polynomial Structure** 



**Polynomial Structure** 





# Signal Training to derive the Memory Polynomial

- <u>Pre-distorter training</u>: Nonlinear coefficients are extracted from the PA input and PA output waveforms (ie – on real physical behavior)
- 2. <u>Copy of PA</u>: The DPD model accurately captures the nonlinearity with memory effects

#### **Memory Polynomial Coefficients**

$$\hat{a} = (U^{H}U)^{-1}U^{H}z$$
$$\hat{a} = [\hat{a}_{10}, \dots, \hat{a}_{K0}, \dots, \hat{a}_{1Q}, \dots, \hat{a}_{KQ}]^{T}$$
$$z = [z(0), z(1), \dots, z(N-1)]^{T}$$





# **Crest Factor Reduction (CFR) Concepts**

- Spectrally efficient wideband RF signals may have PAPR >13dB.
- CFR preconditions the signal to reduce signal peaks without significant signal distortion
- CFR allows the PA to operate more efficiently it is not a linearization technique
- CFR supplements DPD and improves DPD effectiveness
- Without CFR and DPD, a basestation PA must operate at significant back-off from saturated power to maintain linearity. The back-off reduces efficiency

### **Benefits of CFR**

- 1. PAs can operate closer to saturation, for improved efficiency (PAE).
- 2. Output signal still complies with spectral mask and EVM specifications



### **Crest Factor Reduction (CFR) Concepts** V₀ut 7 dB output PAR 1 dB compression (maximum output) reduce Input signal Average power (0 dB point) 13 dB input PAR V<sub>in</sub>

If you can reduce the Peak-to-Average Ratio of the signal, then for a given amplitude Peak, you can raise the Average power (up & to the right, above) with no loss in signal quality.

Thus, CFR enables higher PA efficiency by reducing the back-off, often by 6dB

# **Crest Factor Reduction for Multiple-Carrier Signals**

- Multiple-Carrier Signals (such as GSM, WCDMA, WiMAX) already have high PAPR.
- In the future, they will also include multiple waveforms (ie LTE with 3G WCDMA).
- Therefore CFR will increase in importance for Multi-Carrier PA (MCPA) linearization.



CFR algorithm for multiple carrier signals

- PW (Peak Windowing)-CFR
- NS (Noise-Shaping) -CFR
- PI (Pulse Injection)-CFR

Copyright Agilent Technologies 2010

• PC (Peak Cancellation)-CFR



# CFR for 3GPP LTE DL OFDM Signal

- Controls EVM and band limits in the frequency domain.
  - Constrains constellation errors, to avoid bit errors.
  - Constrains the degradation on individual sub-carriers.
- Allows QPSK sub-carriers to be degraded more than 64 QAM subcarriers.
- Does not degrade reference signals, P-SS and S-SS.
- All control channels (PDCCH, PBCH, PCFICH and PHICH) adopts QPSK threshold.



## LTE CFR (Crest Factor Reduction)



#### **Simulation Results**

LTE Downlink 10MHz, Sampling Rate 61.44MHz, QPSK, EVM threshold 10%

Origin\_PAPR CFR\_PAPR 9.05 6.685





Copyright Agilent Technologies 2010

Agilent Technologies

SystemVue DPD Jinbiao XU May 26, 2010

## **DPD Simulation Workspace**





SystemVue DPD Jinbiao XU May 26, 2010



### LTE DPD simulation for a memoryless nonlinear PA

Copyright Agilent Technologies 2010

71.651

DPD\_PA\_ACLR\_L\_28V[DPD\_PA\_ACLR\_L\_8V[DPD\_PA\_ACLR\_U\_8V[DPD\_PA\_ACLR\_U\_28W]

63.404

64.067

71.497

## LTE DPD simulation for a nonlinear PA with memory





# **DPD Hardware Verification Flowchart**





DPD HW Flowchart consists of 5 steps:

- Step 1 (Create DPD Stimulus) is to download waveform (LTE or User defined) into ESG/MXG.
- Step 2 (Capture DUT Response) is to capture both waveforms before power amplifier and after power amplifier from PSA/MXA/PXA by using VSA89600 software.
- Step 3 (DUT Model Extraction) is to extract PA nonlinear coefficients based on both captured PA input and PA output waveforms and then to verify DPD by using PA nonlinear coefficients.
- Step 4 (DPD Response) is to download the waveform (LTE or User Defined) after predistorter (by using PA nonlinear coefficient from Step 3) into ESG/MXG, this real signal passes through the PA DUT, capture PA output waveform from PSA/MXA/PXA by using VSA89600 software.
- Step 5 (Verify DPD Response) is to show the performance improvement after DPD.



## **DPD Hardware Verification Workspace Structure**

		- 6	🗟 🔄 Step 4 DPD Response
-	DPD_LTE_DL	/	🚊 🛅 Step 4.1 Power Alignment
<u> </u>	🔄 Step 1 Create DPD Stimulus	/	- PowerAlignment (Schematic
	CCDF Measurement	/	PowerAlignment_AM_AM
	CreateDPDStimulus (Schematic)	· · · · · · · · · · · · · · · · · · ·	
	101 CreateDPDStimulus Analysis (CreateDPDStimulus)	/	PowerAlignment_Analysis_I
	CreateDPDStimulus Analysis Data (CreateDPDStimulus Analysis)	/	🖨 😋 Step 4.2 Apply DPD
	A PAPR		
	Step 2 Canture DI IT Response		LTE_DL_DPD (Schematic)
	CantureDLITReconce (Schematic)	/ · · · · ·	101 LTE_DL_DPD_Analysis (LTE
	101 CaptureDUTBespanse (Schematic)	/	
	CaptureDoTResponse Analysis (CaptureDoTResponse)	/	😑 😋 Step 4.3 Capture DPD-PA Outp
<u> </u>	CaptureDUTResponse Analysis_Data (CaptureDUTResponse Analysis)	le la	CaptureDPD-PAOutputData
9(	Step 3 DUT Model Extraction	i de la companya de l	CaptureDPD-PAOutputData
	DPD_NMSE	/	CaptureDPD-PAOutputData
	DPD_PowerAlignment	/ 6	🗈 📹 Step 5 Verify DPD Response
	M DPD_Verification_AM_AM		Step 5.1 Download Waveform
	- Martin DPD_Verification_Spectrum	1	LTE_DL_NoDPD_To_ESG (S
	DUTModelExtraction (Schematic)		LTE_DL_NoDPD_To_ESG_A
	DUTModelExtraction Analysis (DUTModelExtraction)		LTE_DL_NoDPD_To_ESG_A
	DUTModelExtraction Analysis_Data (DUTModelExtraction Analysis)		Step 5.2 Capture PA Output W
	PA AM AM		
	Step 4 DPD Response		
T	E-Step 4.1 Power Alignment		CaptureNODPD-PAOutput
			SpectrumComparison
	E Contractor A 2 Contractor DBD B0 Output Wouldown		SpectrumPlot (Schematic)
<u> </u>	Chan E Marifer DPD Deserves		191 SpectrumPlot Analysis (Spe
<u> </u>	🔄 Step 5 Veniry DPD Response		SpectrumPlotComparison (SpectrumPlotComparison (Spectr
	Emergence Step 5.1 Download waveform (No DPD) to ESG		Step 5.4 EVM Measurements
	Step 5.2 Capture PA Output Waveform (No DPD)		
	E Step 5.3 Spectrum Comparison		EVMMeasurements (Schem
	🖻 🛅 Step 5.4 EVM Measurements		EVMMeasurements Analysis
	🖻 💼 Step 5.5 ACLR Measurements		EVMMeasurements Analysis
			E G Step 5.5 ACLR Measurements
		and the second second	ACLRMeasurements (Scher
		and the second se	101 ACLRMeasurements Analys
			ACLRMeasurements Analys

ic) (PowerAlignment) Data (PowerAlignment\_Analysis) DL\_DPD) ta (LTE\_DL\_DPD\_Analysis) put Waveform a (Schematic) a Analysis (CaptureDPD-PAOutputData) a Analysis\_Data (CaptureDPD-PAOutputData Analysis) (No DPD) to ESG Schematic) Analysis (LTE\_DL\_NoDPD\_To\_ESG) Analysis\_Data (LTE\_DL\_NoDPD\_To\_ESG\_Analysis) Vaveform (No DPD) )ata (Schematic) Data Analysis (CaptureNoDPD-PAOutputData) )ata Analysis\_Data (CaptureNoDPD-PAOutputData Analysis) ectrumPlot) SpectrumPlot Analysis) natic) is (EVMMeasurements) is\_Data (EVMMeasurements Analysis)

- matic)
- sis (ACLRMeasurements)
- sis\_Data (ACLRMeasurements Analysis)
- 🚟 After\_PA\_ACLR
- AfterDPD\_PA\_ACLR
- Original\_ACLR

# **DPD Hardware Verification Platform**

### 1. PA input signal capture



### 2. PA output signal capture





# **DPD Hardware Verification – LTE (Step 1)**



🤪 DPD 🚽 2: Capture DUT Response 1: Create DPD Stimulus 3: DUT Model Extraction 4: DPD Response 5: Verify DPD response LTE Parameters Cyclic Prefix (CP) Type Bandwidth Oversampling Option Normal (Nsc: 12 | Nsymb: 7) 2.0e9 3: BW 10 MHz (50 RB) FCarrier Hz Ratio 4 Extended (Nsc: 12 | Nsymb: 6) CFREnable 0.0000165 Clipping Threshold 64QAM\_EVMThreshold 0.1 QPSK\_EVMThreshold 0.1 16QAM\_EVMThreshold 0.1 Mapping Type (Modulation Scheme) Subframe 0 1 2 3 4 5 6 7 8 9 OPSK -OPSK 🐱 OPSK 🐱 OPSK 🐱 OPSK 🐱 OPSK 🐱 QPSK 👻 QPSK 🐱 QPSK 🗸 CW OPSK -Current UE: 1 Edit User Mapping Prev UE Next UE **Download Parameters** -2 146.208.175.2 RFPower dBm ¥ PrimAddress 0 30 TimeStart ms 4 ms TimeStop LTE DL Source MXG/ESG Go To ESG Web Control Download Waveform CCDF 6.85698777 PAPR

The CFR must be enable in LTE source.

LTE paramters (such as bandwidth, Resource Block allocation and etc) can be set.

The download waveform transmit power, length also can be set.



18



# **DPD Hardware Verification – LTE (Step 2)**





Firstly, connect the ESG directly with the PSA/PXA and click the "Capture Waveform" button in the "Capture PA Input" panel in the GUI. The captured signal is the input of the PA DUT.

Then, connect the ESG with the DUT, and then connect the DUT with the PSA/PXA and click the "Capture Waveform" button in the "Capture PA Output" panel in the GUI. The captured signal is the output of the PA DUT.

These I/Q files are stored for further usage.



# **DPD Hardware Verification – LTE (Step 3)**



# **DPD Hardware Verification – LTE (Step 4)**



This step is to apply the DPD model extracted in Step 3. The generated LTE downlink signal is firstly pre-distorted by the extracted model, and then downloaded into the ESG.







Copyright Agilent Technologies 2010



SystemVue DPD Jinbiao XU May 26, 2010

# **DPD Hardware Verification – LTE (Step 5)**



This step is to verify the performances of the DPD (including spectrums of the DUT output signal w/ and w/o DPD, EVM and ACLR).



🥥 DPD									
1: Create	DPD Stimulus	2: Ca	apture DUT Response	3: DUT Model E	traction 4: DPD Respon	se 5: Verify [	OPD Response		
Download	Parameters —								
RFPov	wer -4.963	dBm	~	Prim/	Address 146.208.175.2	]			
Time St	itart 0	ms	~	Tin	ne Stop 30 ms	*			
LTE DL Source					MXG/ESG This step is to download the original signal (without DPD) w the same RF power as step 4. 1 may also use the downloaded waveform in step 1 and change the power in MXG/ESG.				
$ \longrightarrow  \longrightarrow $									
Capture Waveform									
- Show Res	ults			Captur	e Waveform				
Show Res	ults Spectrum		EVM	Captur	e Waveform				
Show Res	Spectrum		EVM	Captur ACL	e Waveform		Driginal	After	PA
- Show Res	sults Spectrum	M (	EvM dB)	Captur ACL Index	AfterDPD_PA	(	Driginal	After_ -18.5	.PA
- Show Resi	sults Spectrum	M (	EVM dB)	Captur ACL Index 1 2	AfterDPD_PA -19.443 -18.84	( - -	Driginal 19.382 18.844	After_ -18.( -18.(	P/ 57
- Show Res	EV	M ( .R (	еум dB) (dB)	Captur ACL Index 1 2	AfterDPD_PA -19.443 -18.84	( -	Driginal 19.382 18.844	After_ -18.5 -18.0	
- Show Res	EVI ACL	M ( .R ( 3W (	■EVM dB) (dB) Driginal_AC	Captur ACL Index 1 2 LR_L_BW	AfterDPD_PA -19.443 -18.84 Original_ACLR	 	Driginal 19.382 18.844 Original	After_ -18.( -18.(	P/ 57: 07
-Show Res	EVI ACL	<b>M (</b> . <b>R (</b> . <b>R</b> ( .79	■EVM dB) (dB) Driginal_AC	Captur ACL Index 1 2 LR_L_BW 50.653	AfterDPD_PA -19.443 -18.84 Original_ACLR	U_BW 51.252	Driginal 19.382 18.844 Original	After_ -18.( -18.( I_ACLR_U_	.P4 577 07
Show Res	EVI ACL	<b>M (</b> . <b>R (</b> . <b>R</b> ( 3W ( 179	■ <b>dB)</b> ( <b>dB)</b> Driginal_AC	Captur ACL Index 1 2 LR_L_BW 50.653 BW	AfterDPD_PA -19.443 -18.84 Original_ACLR	U_BW 51.252	Driginal 19.382 18.844 Original	After_ -18.6 -18.0 I_ACLR_U_ 1_R_U_2BW	P/ 57: 07 2E
Show Res	EV	M ( .R ( 3VV ( 179 F 307	■ dB) (dB) Driginal_AC PA_ACLR_I	Captur ACL Index 1 2 LR_L_BW 50.653 BW	AfterDPD_PA -19.443 -18.84 Original_ACLR PA_ACLR_U_	U_BW 51.252 BW 38.361	Driginal 19.382 18.844 Original PA_AC	After_ -18.9 -18.0 I_ACLR_U_ !LR_U_2BW	P/ 57; 07 2E 53 /
Show Res	EV ACL .R_L_2E .2BW 51.3	<b>M (</b> . <b>R</b> ( 3VV ( 179 ) 307 )	CB) (dB) (dB) Driginal_AC	Captur ACL Index 1 2 LR_L_BW 50.653 BW 38.244	AfterDPD_PA -19.443 -18.84 Original_ACLR PA_ACLR_U_	U_BW 51.252 BW 38.361	Driginal 19.382 18.844 Original PA_AC	After_ -18.( -18.( I_ACLR_U_ ! LR_U_2BW	P/ 57; 07 2E 53. /
show Res	EVI ACL 	<b>M</b> (1 . <b>R</b> (1 3VV (1 179 F 307 2BV [1	<b>dB)</b> ( <b>dB)</b> Driginal_AC	Captur ACL Index 1 2 LR_L_BW 50.653 BW 38.244 CLR_L_BW	AfterDPD_PA -19.443 -18.84 Original_ACLR PA_ACLR_U_ DPD_PA_ACL	U_BW 51.252 BW 38.361 R_U_BW	Driginal 19.382 18.844 Original PA_AC	After_ -18.( -18.( I_ACLR_U_ ! !LR_U_2BW	P4 577 577 577 577 577 577 577 577



# Hardware Verification Results of Doherty PA



### References

- 1. Lei Ding, Zhou G.T., Morgan D.R., Zhengxiang Ma, Kenney J.S., Jaehyeong Kim, Giardina C.R., "A robust digital baseband predistorter constructed using memory polynomials", <u>Communications, IEEE Transactions on</u>, Jan. 2004, Volume: 52, Issue:1, page 159-165.
- 2. Lei Ding, "*Digital Predistortion of Power Amplifiers for Wireless Applications*", PhD Thesis, March 2004.
- 3. Roland Sperlich, "Adaptive Power Amplifier Linearization by Digital Pre-Distortion with Narrowband Feedback using Genetic Algorithms", PhD Thesis, 2005.
- 4. Helaoui, M. Boumaiza, S. Ghazel, A. Ghannouchi, F.M., "*Power and efficiency enhancement of 3G multicarrier amplifiers using digital signal processing with experimental validation*", <u>Microwave Theory and Techniques, IEEE Transactions on</u>, June 2006, Volume: 54, Issue: 4, Part 1, page 1396-1404.
- 5. H. A.Suraweera, K. R. Panta, M. Feramez and J. Armstrong, "*OFDM peak-to-average power reduction scheme with spectral masking*," Proc. Symp. on Communication Systems, Networks and Digital Signal Processing, pp.164-167, July 2004.
- 6. Zhao, Chunming; Baxley, Robert J.; Zhou, G. Tong; Boppana, Deepak; Kenney, J. Stevenson, "*Constrained Clipping for Crest Factor Reduction in Multiple-user OFDM*", Radio and Wireless Symposium, 2007 IEEE Volume , Issue , 9-11 Jan. 2007 Page(s):341- 344.
- 7. Olli Vaananen, "Digital Modulators with Crest Factor Reduction Techniques", PhD Thesis, 2006
- 8. Boumaiza, et a, "On the RF/DSP Design for Efficiency of OFDM Transmitters", *IEEE Transactions on Microwave Theory and Techniques*, Vol. 53, No. 7, July 2005, pp 2355-2361.
- 9. Boumaiza, Slim, *"Advanced Memory Polynomial Linearization Techniques*," IMS2009 Workshop WMC (Boston, MA), June 2009.
- 10. Amplifier Pre-Distortion Linearization and Modeling Using X-Parameters, Agilent EEsof EDA



